AUTOMATED INTEGRATION OF SIMULINK MODELS INTO VIRTUAL PLATFORMS

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MATLAB EXPO
JUNE 27TH, 2017
MUNICH, GERMANY

This work has been funded by the German Federal Ministry for Education and Research (BMBF) under the grant 01IS13022A (project EffektiV). The content of this publication lies within the responsibility of the authors.
Agenda

The Application: Automotive Mixed-Signal ASICs

The Current Workflow and its Challenges

The Improved Workflow

Summary & Conclusion
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1. The Application: Automotive Mixed-Signal ASICs
2. The Current Workflow and its Challenges
3. The Improved Workflow
4. Summary & Conclusion
Integration of Simulink Models into Virtual Platforms
Automotive Mixed-Signal ASICs

▼ Bosch accelerates progress of automotive technology with continued innovations like ESP or autonomous driving solutions

▼ Integral part for these solutions are automotive sensors

▼ Example: Inertial sensor system for ESP
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Automotive Mixed-Signal ASICs

- Heterogeneous SoC:
  - Analog Hardware
  - Digital Non-Programmable Hardware
  - Processors

- System-in-Package (SiP)

- Sensor

Source: Karsten Funk
Integration of Simulink Models into Virtual Platforms
Sensor ASIC – Architecture Example

- Signal path for sensor signal processing

- General Purpose Processor (GPP) subsystem for
  - safety monitoring
  - communication protocols
  - etc.

- Several interfaces

- On-Chip Architecture
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Sensor ASIC – Signal Path Example
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Current Workflow - IP-XACT-Centric Tool Environment

- IP-XACT description as single source

- Generation of various design, test and documentation outputs

- Ensures consistency throughout the whole design flow
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Current Workflow - IP-XACT-Centric VP Generation

- Description of architecture and register interfaces in IP-XACT
- Automated generation of VP architectures and TLM register interfaces
- Signal processing algorithm design using Model-Based Design
- Manual behavioural description of control- and signal-flow oriented designs
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Architecture Design - Magillem® IP-XACT Packager (MIP)

- Design of On-Chip Architecture in Magillem® IP-XACT Packager
- Saved as IP-XACT Design description
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Register Interface Design - Magillem® Register View (MRV)

- Design of register interfaces in Magillem® Register View
- Saved as IP-XACT Component description
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Current Workflow - IP-XACT-Centric VP Generation

Automated generation of VP architectures and TLM register interfaces
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Virtual Platforms (VP)

- SoC architecture-centric
- Highspeed pre-silicon development environment
- Abstracting communication interfaces through Transaction Level Modelling (TLM)

Benefits
- SoC concept validation and architectural exploration
- Concurrent SW and HW development
- Validation of HW/SW interfaces
- Optimization of SW
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System Simulation and SW Dev. in Synopsys® Virtualizer™

- Tool for construction and simulation of Virtual Prototypes
- Large module library
- Comprehensive debugging capabilities
- Export of development kits for SW development
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Current Workflow - IP-XACT-Centric VP Generation

Signal processing algorithm design using Model-Based Design
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Model-Based Design (MBD)

- Algorithm-centric
- Signal flow-oriented multi-domain simulation
  - Differential equation, transfer function, physical network level
  - Time-continuous, time-discrete
  - Value-continuous, value-discrete

Benefits
- Mathematical algorithm design
- Early verification of its functional correctness and performance in its environment
- Implementation through automatic code generation
Example: Lowpass Filter Design with DSP System Toolbox™

Specification:
- Filter response: FIR
- Design Method: Equiripple
- 6dB-cutoff frequency: 0.25
- Stopband attenuation: 60 dB
- Passband ripple: 1 dB
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Signal-Flow-based Simulation with Simulink®

Time domain:

Frequency domain:
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Gap Analysis

- **Benefits of Model-Based Design**
  - Verified algorithm meeting signal processing characteristics

- **Workflow Gap**
  - Manual behavioural description of algorithm
  - Manual integration into SystemC TLM wrapper

- **Potential Issue**
  - Mismatch between manual behavioural description and implementation
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Gap Analysis

Solution:

- Automatic generation of SystemC TLM component
  - Behavioural algorithmic model
  - Integration in SystemC TLM wrapper
- IP-XACT register definition as input
- Support of SCML register
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Algorithm Design & Model Generation

- Extended Model-Based Design Workflow
  - Model Generation
- Additional code generation targets
  - Virtual platforms (e.g. SystemC TLM 2.0)
  - Verification environments (e.g. SystemVerilog DPI-C)
- Benefits
  - Integrated, automated workflow
  - Functional equivalence between ..
    - Algorithm design
    - Virtual Platform model
    - Algorithm implementation
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Algorithm Design & Model Generation

- **Algorithm Design**
  - Mathematical representation
  - Multi-domain simulation environment
    - Early algorithm verification within its environment

- **Model Generation**
  - Automatic code generation (SystemC TLM)
  - IP-XACT register description as input
  - Behavioural description integrated in SystemC TLM wrapper
  - Self-testing SystemC TLM testbench
  - IP-XACT register description as output
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Model Generation - IP-XACT Register Mapping (I/O, Parameters)

**Input: IP-XACT Register Mapping**

```
<spirit:memoryMap>
  <spirit:name>memorymap_bus</spirit:name>
  <spirit:addressBlock>
    <spirit:name>BusInterface_AddressBlock</spirit:name>
    <spirit:baseAddress spirit:id="subsystem_TLM_base_address_output" spirit:range spirit:resolve="immediate">0x100</spirit:range>
    <spirit:width>64</spirit:width>
  </spirit:addressBlock>
  ...more memory maps...
</spirit:memoryMap>

<spirit:register>
  <spirit:name>ACCI_Out</spirit:name>
  <spirit:addressOffset>0x00</spirit:addressOffset>
  ...more register details...
</spirit:register>

<spirit:parameter>
  <spirit:name>MWMapOutput</spirit:name>
  <spirit:value>sym_Hlp4</spirit:value>
</spirit:parameter>
```

**Interface mapping between IP-XACT and Simulink**

**SCML Register Support**

Import IP-XACT File

IP-XACT file: C:\04_SBX_ROOT\SystemC_TLM\Signal_Path.xml

Implement memory map with SCML
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Model Generation - SystemC TLM/SCML Adaptor Architecture
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Integration and Simulation - Manual Import of SystemC Module
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Integration and Simulation - SystemC Module in Synopsys® Virtualizer™
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Integration and Simulation – Simulation in Synopsys® VPExplorer
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Summary – Bosch Workflow

- Architecture Design
- Register Design
- Control-Flow Design
- Algorithm Design (MBD)
- ASIC Requirements

- VP Architecture Generation
- SystemC TLM Wrapper Gen.
- Manual behav. Description

- MATLAB®, Simulink®, DSP System Toolbox™
- Simulink® Coder™ / Embedded Coder®, HDL Verifier™
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Summary & Conclusion

▶ Developed method:
  Automated integration of Simulink signal processing behaviour modules into Virtual Platforms

▶ Generated artefacts:
  ▶ Functional core
  ▶ SystemC TLM2.0 Wrapper with SCML registers based on IP-XACT description
  ▶ Code connecting wrapper and functional core

▶ Benefits:
  ▶ Increase of efficiency for integration signal processing behaviour into VPs
  ▶ Earlier availability of functional VPs of signal processing ASICs
  ▶ Inherent consistency between Simulink model and VP
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