MATLAB EXPO

2024.06.11 | 그랜드 인터컨티넨탈 서울 파르나스

MATLAB을 이용한 SerDes PHY의 IBIS-AMI Model 생성 및 호환성 검증

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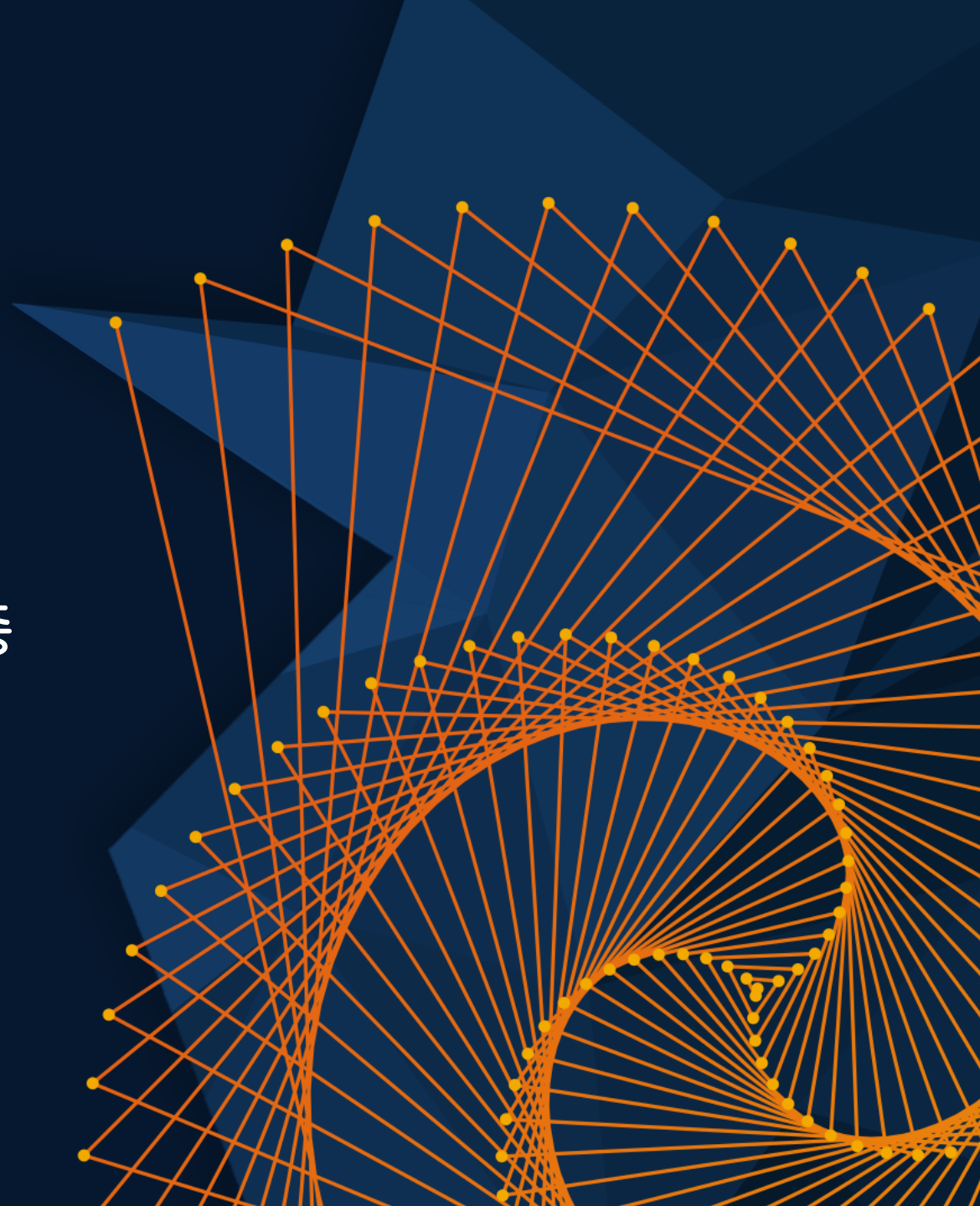
MathWorks

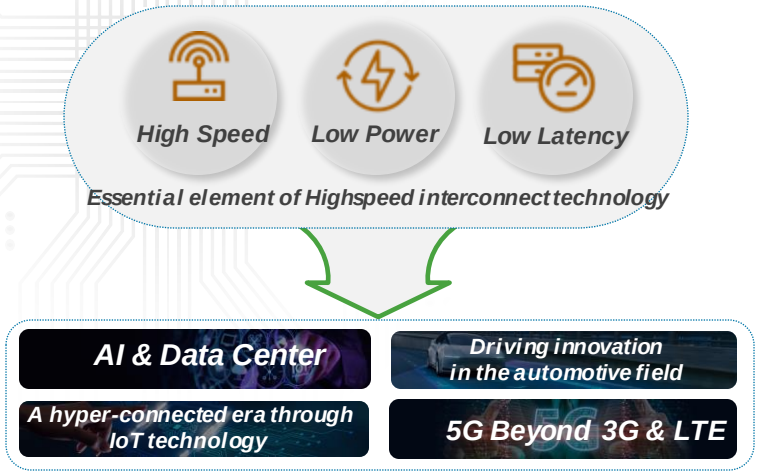


About Qualitas

Connect the World through High-Speed Interconnection

Qualitas Semiconductor is a leading semiconductor design company in the IP and IC market based in Korea. Renowned for our expertise in high-speed interfaces globally, we focus on crafting interconnect PHYs that seamlessly integrate analog and digital signals. As a fabless company, we specialize in providing comprehensive high-speed interconnect solutions required for complex and massive data computations in various fields, including AI, autonomous driving, data centers, AR and VR.

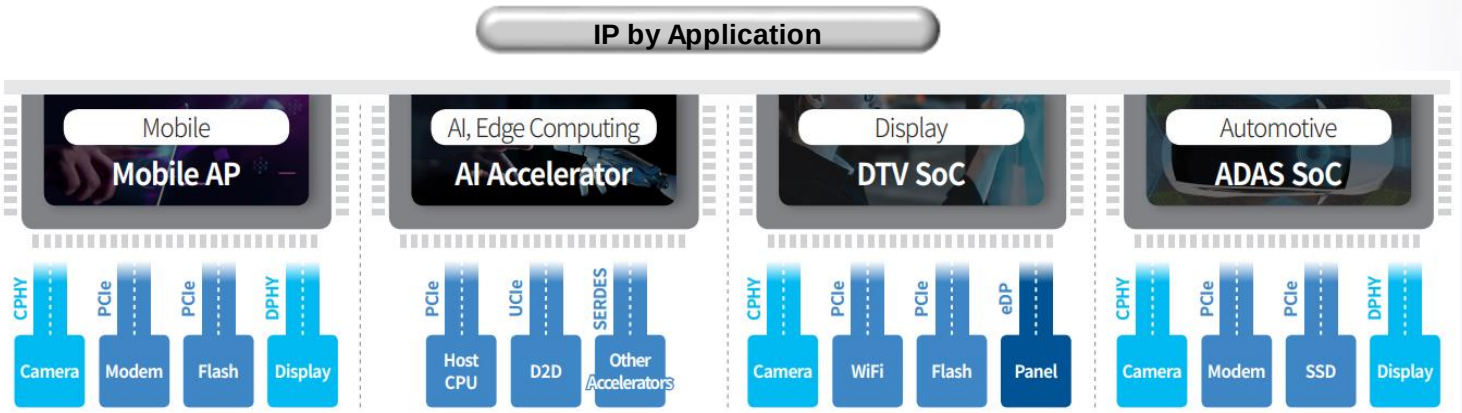
"We provide High-speed Interconnect Total Solution"



About Qualitas – Key Solutions

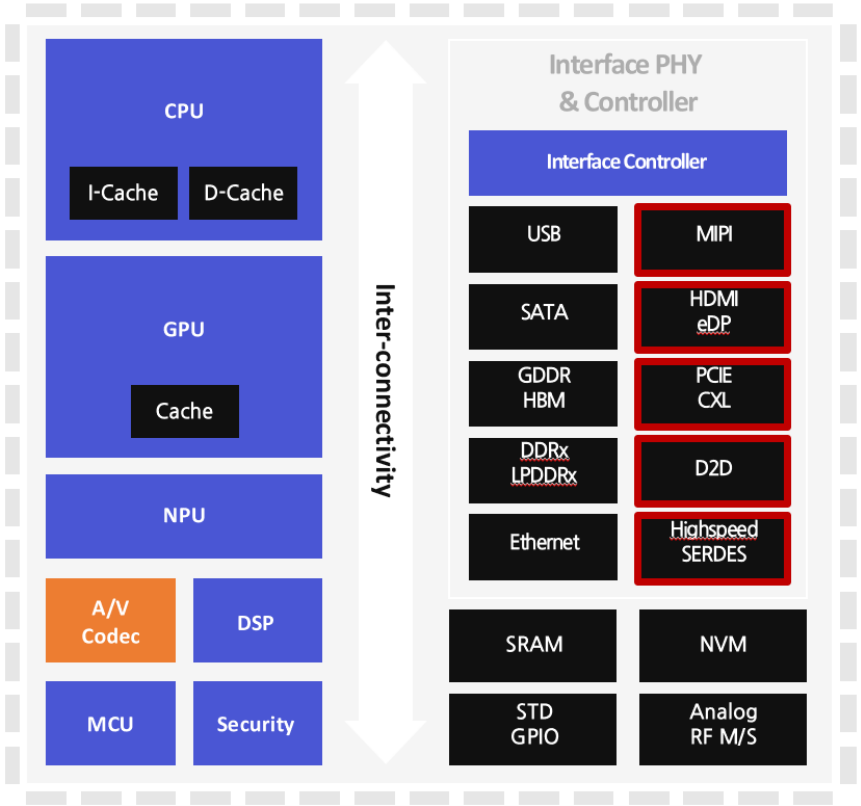
Qualitas specializes in providing *SERDES, PCIe, MIPI, Display IP and Chiplet solutions*

- Leading the High-speed interface IP Market as a key partner of Samsung Electronics Foundry
- Robust Design capabilities for the FinFET process
  - Rich experience with advanced nodes (28, 14, 8, 5, 4nm in Samsung Foundry)
  - Early access to new processes (IP design for 3nm/2nm GAAFET planned in 2025)
- Our IP solutions offer optimized performance and lower power consumption resulting in more efficient processing and cost savings



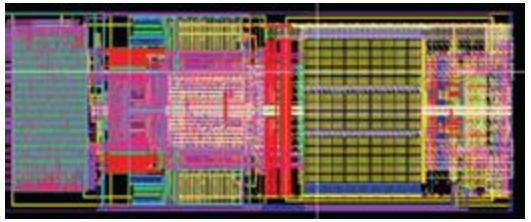
About Qualitas – Key Solutions Cont'

Hardmacro IP
Softmacro IP
providing fast and reliable performance with predictable quality



Hardmacro IP

- Blocks that are generated using a full custom design methodology and imported into the physical design database

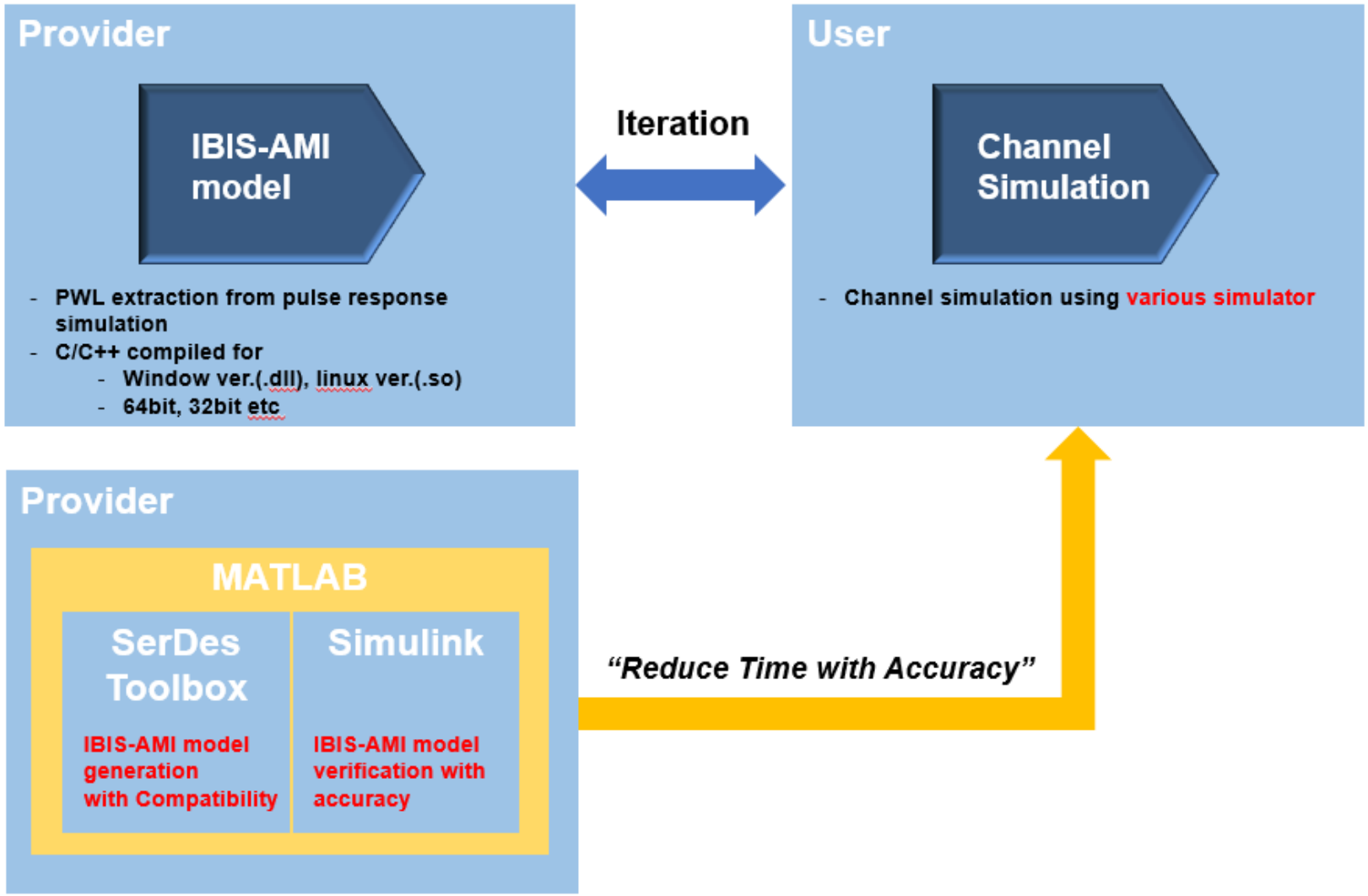


Softmacro IP

- A subunit of a chip and are high-level abstractions defined at the RTL or gate level, which are not tied to a specific technology or process

Contents

Key takeaways



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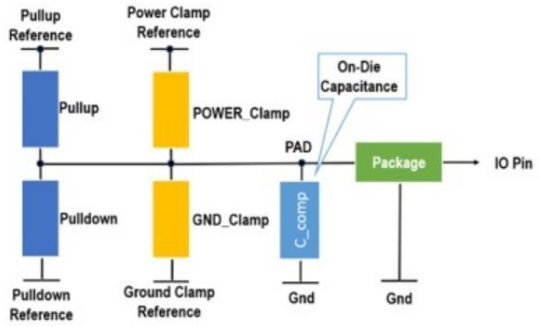
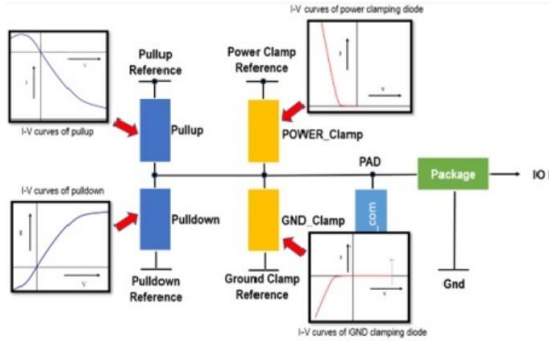
What are IBIS(Input/Output Buffer Information Specification) models?



IBIS output model



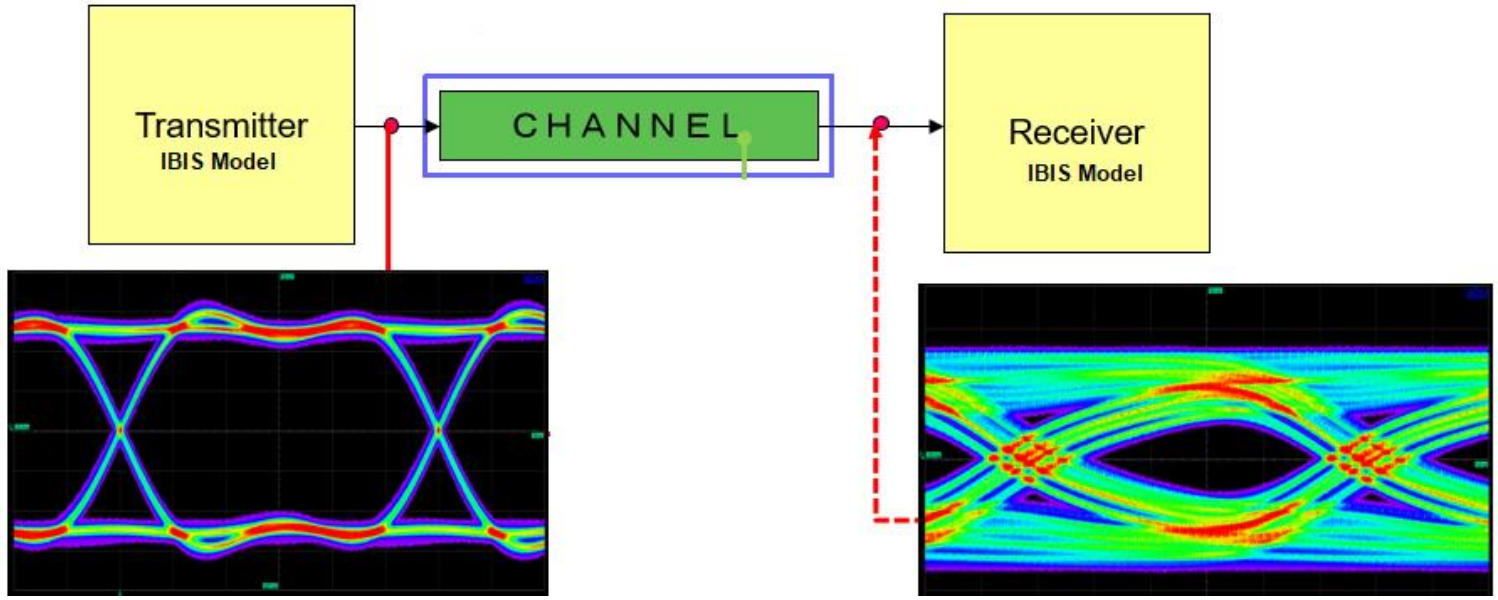
I-V Curve

```
C_comp      0.4pF   0.39pF   0.41pF

[Pullup]
|Voltage    I(typ)  I(min)  I(max)
-0.8V       20mA    20mA    20mA
-0.4V       10mA    10mA    10mA
0V          0.0mA   0.0mA   0.0mA
0.4V        -10mA   -10mA   -10mA
0.8V        -20mA   -20mA   -20mA

[Rising Waveform]
|time        V(typ)        V(min)        V(max)
0.0ps       0.533V        0.507V        0.56V
50.0ps      0.533V        0.507V        0.56V
150.0ps     1.20V         1.14V         1.26V
160.0ps     1.20V         1.14V         1.26V
```

V-T table

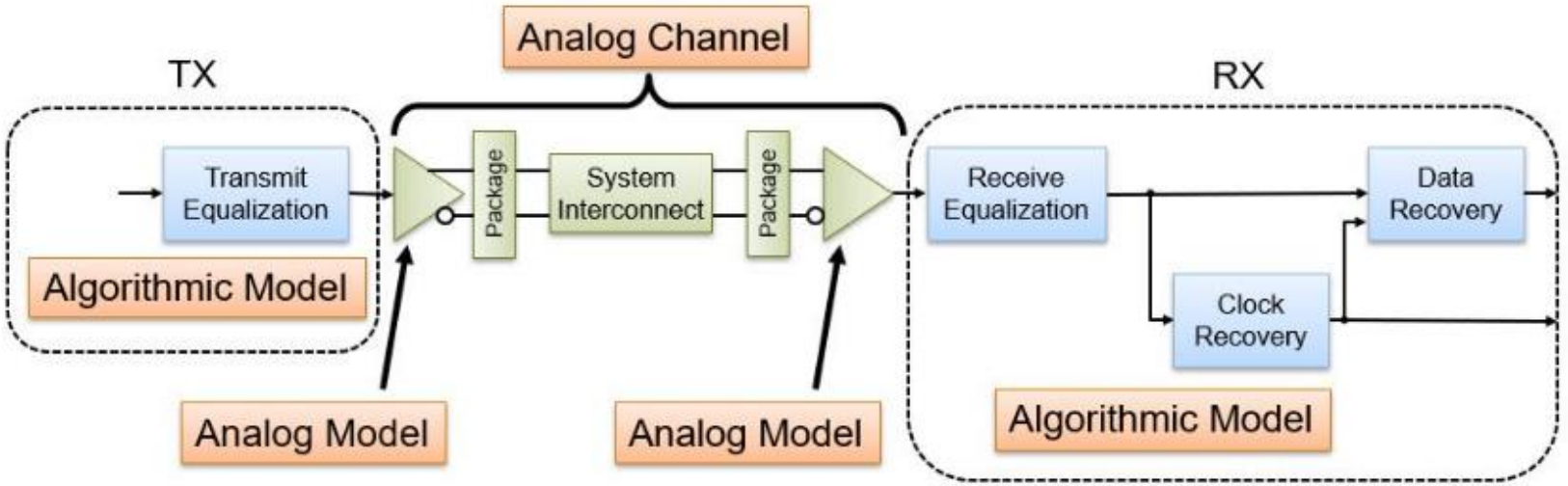
How are IBIS models used?

- Used for SI(Signal Integrity) simulation due to channel loss
- Pros.
  - Accurate model based on full circuit simulation with model parameter
  - Faster than SPICE simulation
- Cons.
  - It is not applicable for complex SerDes system using FFE, DFE, CTLE, CDR etc.



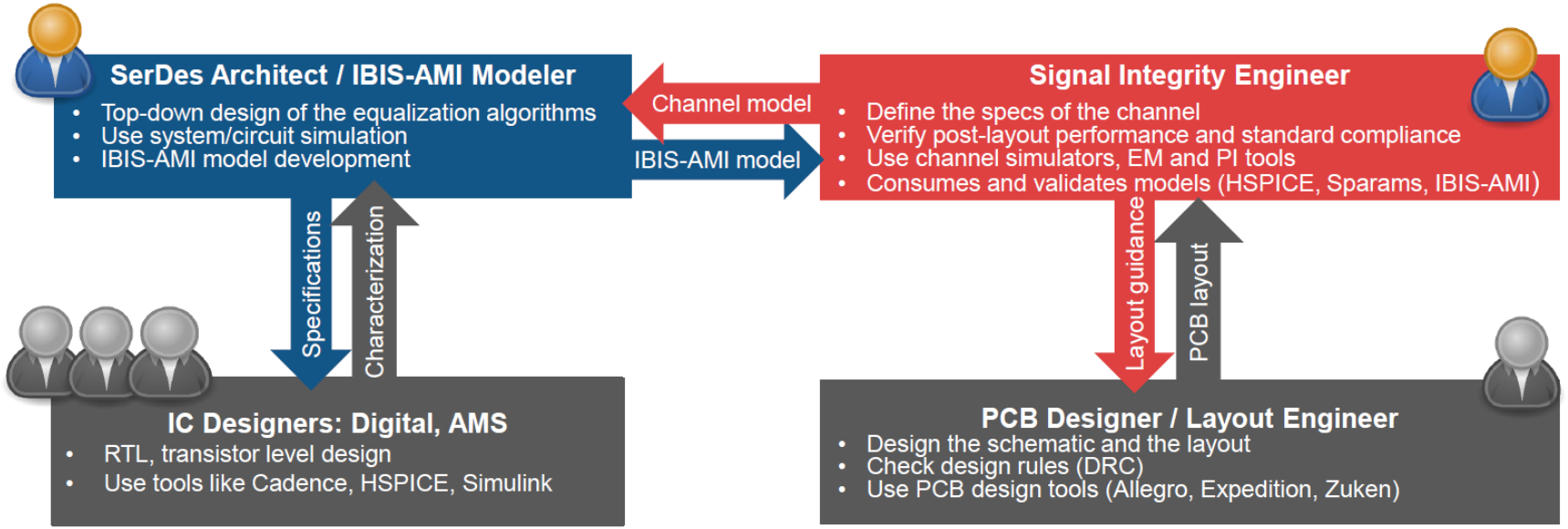
What are IBIS-AMI (Algorithmic Modeling Interface) models?

- IBIS-AMI was developed and was initially approved as part of the IBIS 5.0 Specification
- AMI model is useful for a high-speed serial link's performance with an eye diagram and BER



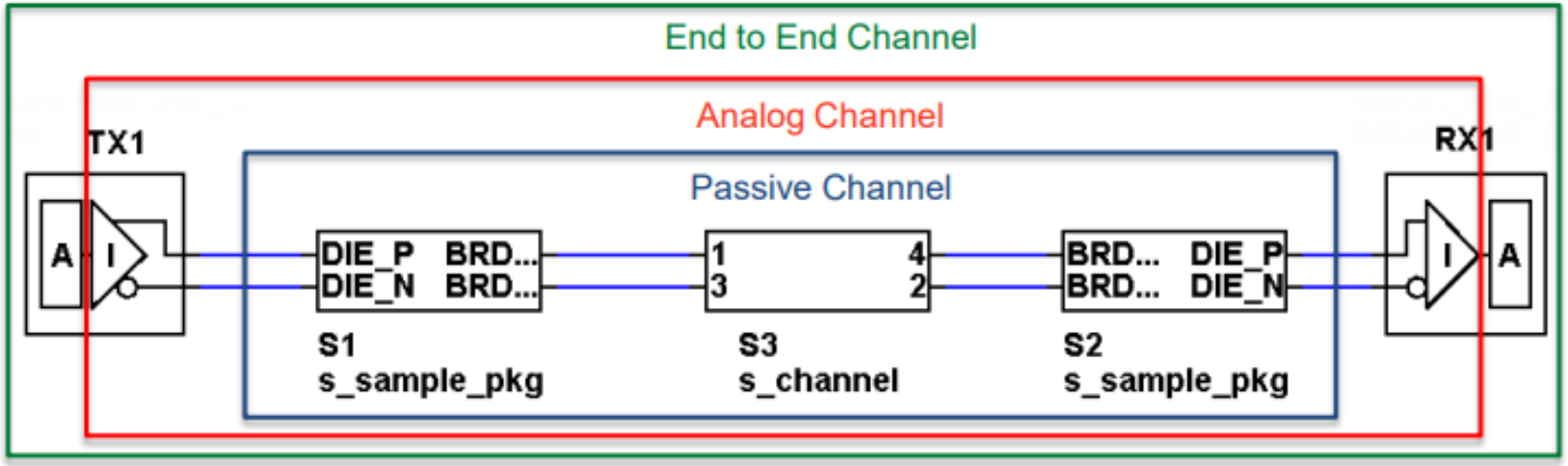
Why using IBIS-AMI model? (1/2)

• SerDes and SI Design and verification workflow

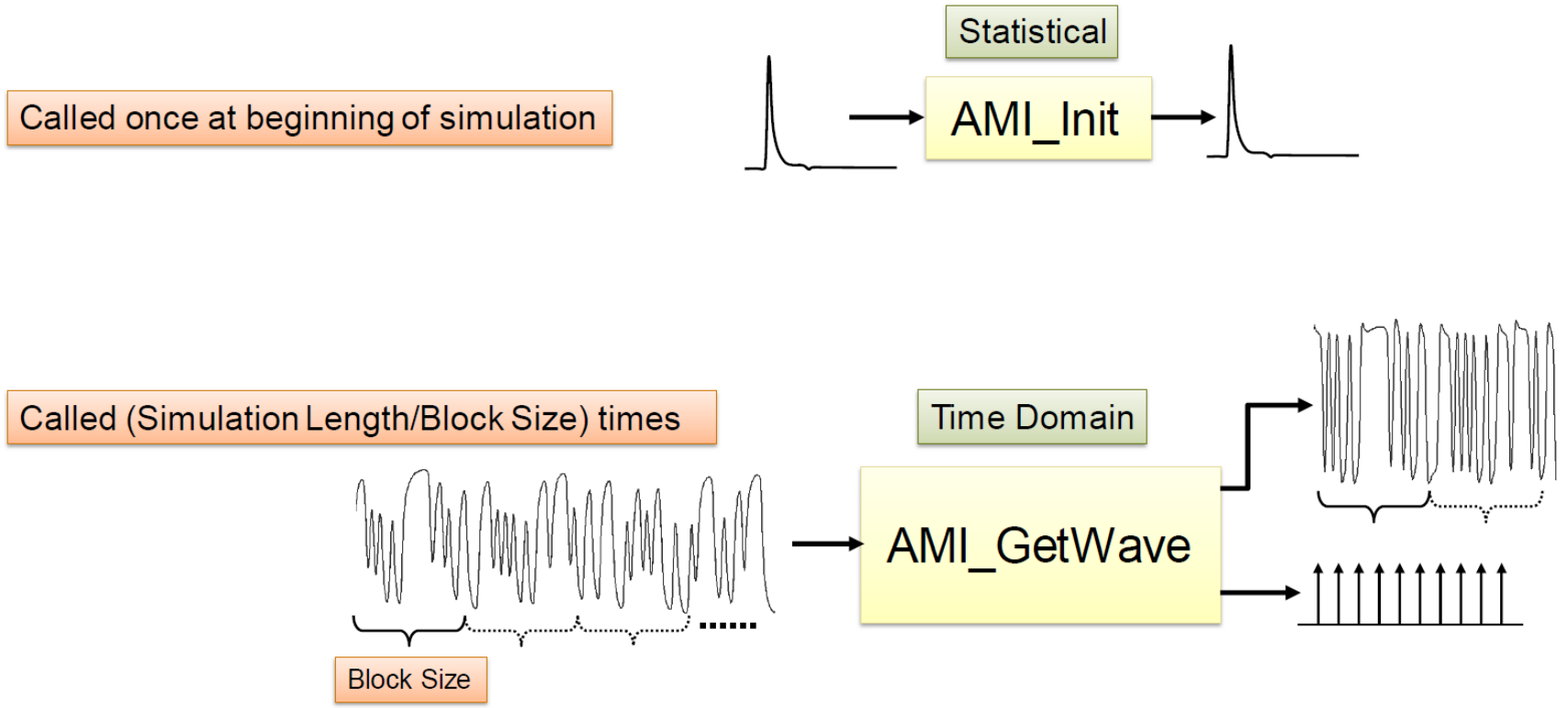


Why using IBIS-AMI model? (2/2)

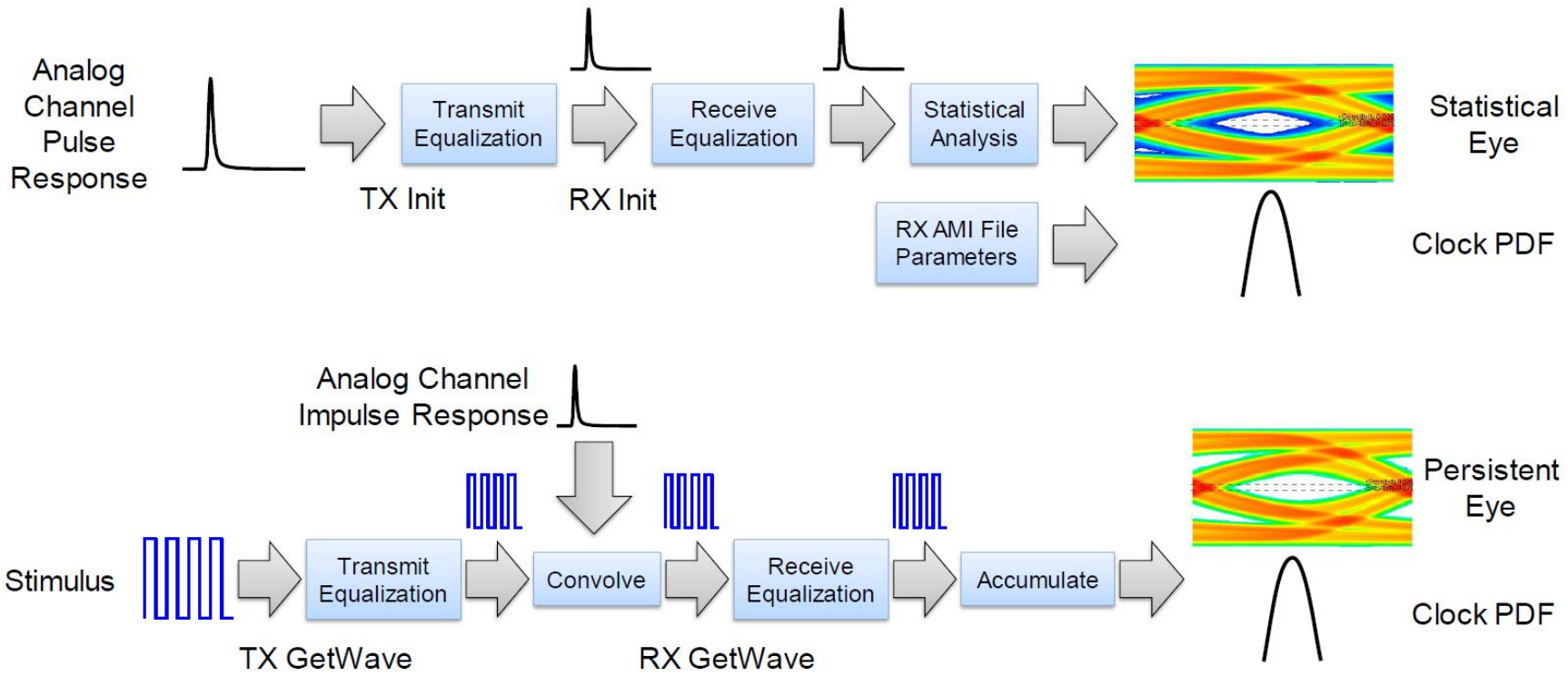
- Fast end-to-end channel simulations with good accuracy
- With IBIS-AMI models and channel simulator, millions of bits can be simulated
  - Effects of ISI
  - Jitter (RJ, DJ)
  - Cross-channel interference and more



IBIS-AMI model : AMI_Init vs. AMI_GetWave



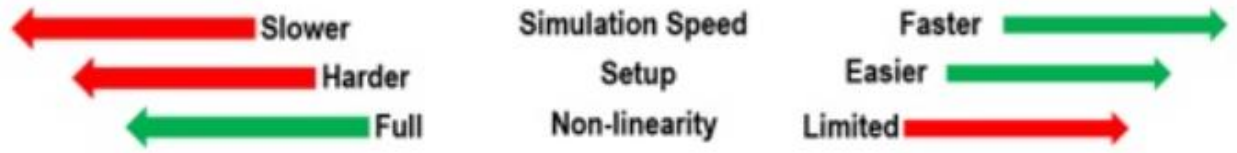
IBIS-AMI model : Statistical vs. Time Domain (1/2)



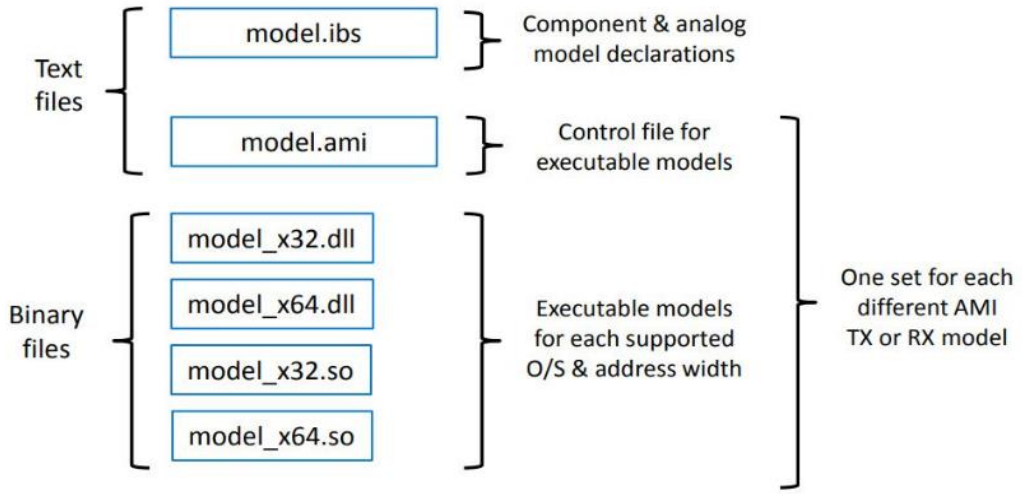
IBIS-AMI model : Statistical vs. Time Domain (2/2)

- Time Domain (Bit-by-Bit) simulation
  - BER extrapolation typically used below 10^(-5)
- Statistical Simulation
  - Used when TX/RX AMI models are LTI
  - The entire system is represented by its impulse response
  - Convenient for a quick analysis, but most practical systems have an RX model that is NLTV

	Traditional IBIS flow: SPICE/Transient Simulation	IBIS-AMI flow: Time Domain (Bit-by-bit) Simulation	IBIS-AMI flow: Statistical Simulation
Technology	Nodal analysis of Kirchoff's current laws	Superposition of single-bit response	Calculations based on impulse response
BER floor in one minute simulation	~10^{-2}	~10^{-5}	~10^{-18} or lower
Applicability & Assumption	Analog & channel : NLTV Tx/Rx : NLTV NLTV = non-linear and/or time varying	Analog & channel : LTI Tx/Rx : NLTV	Analog & channel : LTI Tx/Rx : LTI LTI = linear and time invariant



IBIS-AMI model : Files

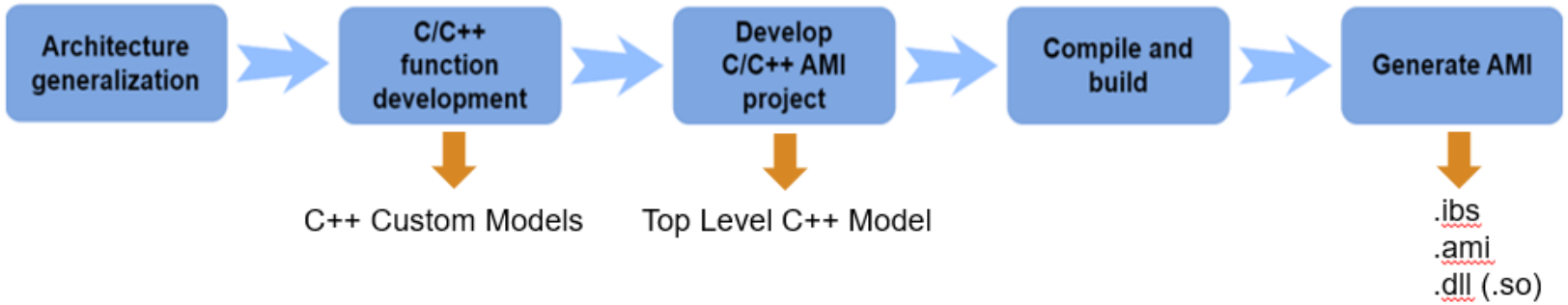



```
(IBIS_AMI_Tx
   (Description "Generic transmitter model")

   (Reserved_Parameters
      (AMI_Version (Usage Info)(Type String)(Value "6.0"))
      (Ignore_Bits (Usage Info)(Type Integer)(Default 4)(Description "Ignore four bits."))
      (Max_Init_Aggressors (Usage Info)(Type Integer)(Default 25)(Description "# of aggressors.")
      (Init_Returns_Impulse (Usage Info)(Type Boolean)(Default True)
         (Description "Impulse & parameters_out returned.")
      )
      (GetWave_Exists (Usage Info)(Type Boolean)(Default True)
         (Description "GetWave is well and truly provided.")
      )
    ) | End Reserved_Parameters

   (Model_Specific
      (tap_filter (Description "Array of transmit de-emphasis tap weights.")
         (-1 (Usage InOut)(Type Tap)(Range 0.0 -1.0 1.0)(Description "Pre-cursor tap weight."))
         (0  (Usage InOut)(Type Tap)(Range 1.0 -1.0 1.0)(Description "Main tap weight."))
         (1  (Usage InOut)(Type Tap)(Range 0.0 -1.0 1.0)(Description "1st post-cursor tap."))
         (2  (Usage InOut)(Type Tap)(Range 0.0 -1.0 1.0)(Description "2nd post-cursor tap."))
      ) | End tap_filter
   ) | End Model_Specific

) | End IBIS_AMI_Tx
```

Contents

IBIS-AMI model Generation

- Algorithmic model is a compiled executable
- AMI model development requires many skills :
  - Master C/C++ coding skills
  - Guarantee coding compatibility across platforms
  - Compile and link program both Windows and Linux



IBIS-AMI model Compatibility

IBIS-AMI model Provider

- Did I write the code that is compatible with all platform/OSs and compilers?
- Who puts everything together into an IBIS file:
- Did I mess up 64bits and 32bits dll/so files in the IBIS file?

IBIS-AMI model User

- Why doesn't this AMI model support my OS? Did I do anything wrong with them?

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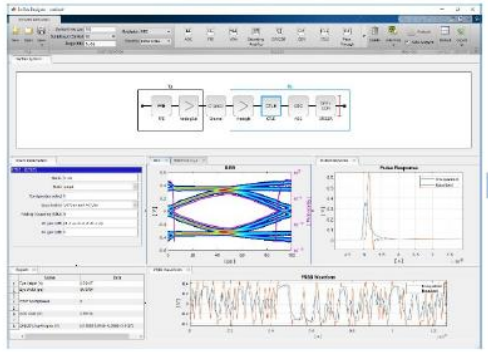
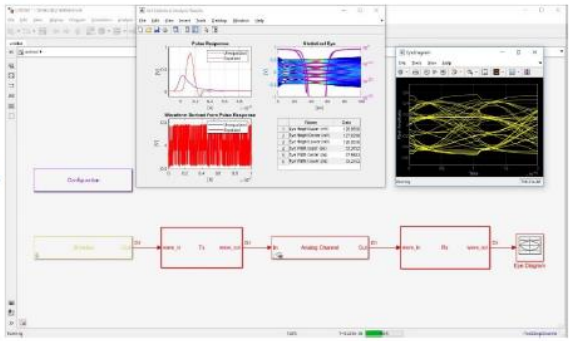
IBIS-AMI model Generation and Verification workflow using MATLAB

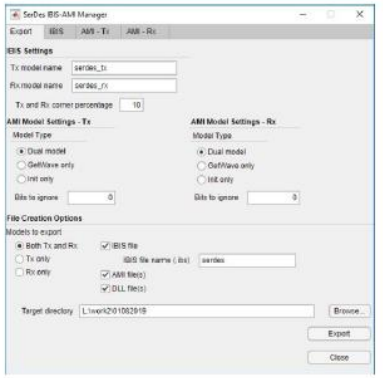
Floorplan



Architectural design

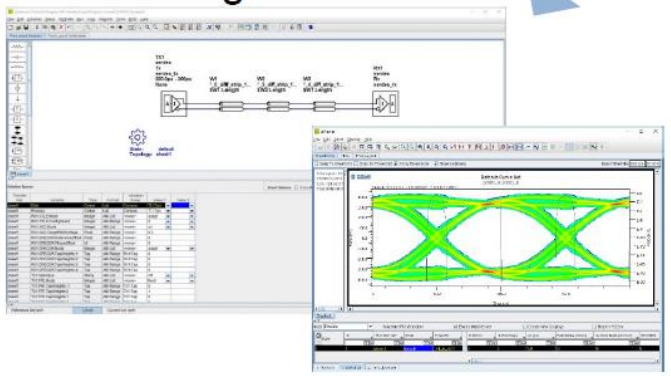


IBIS-AMI model generation



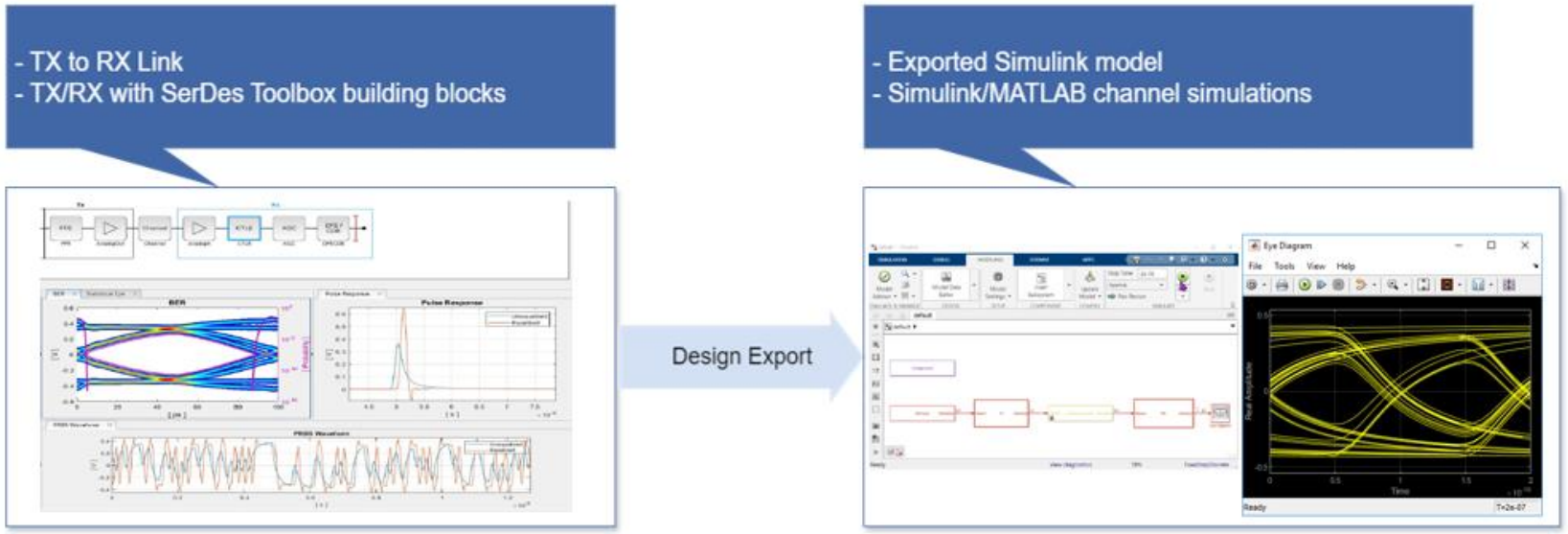
Debug

Regression



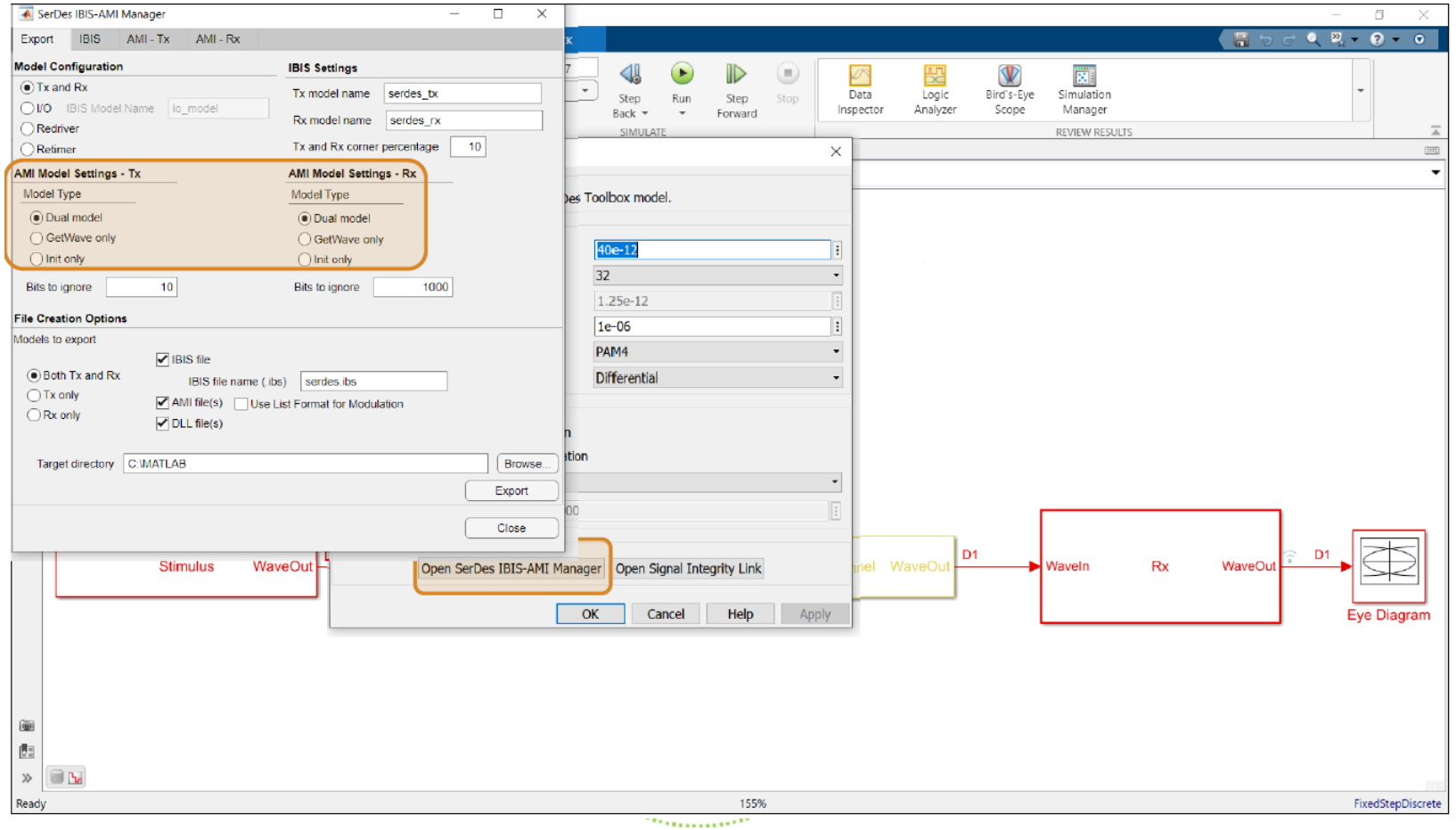
IBIS-AMI model generation (1/3)

- TX & RX with SerDes Toolbox building blocks
- Exported Simulink model and channel simulation



IBIS-AMI model generation (2/3)

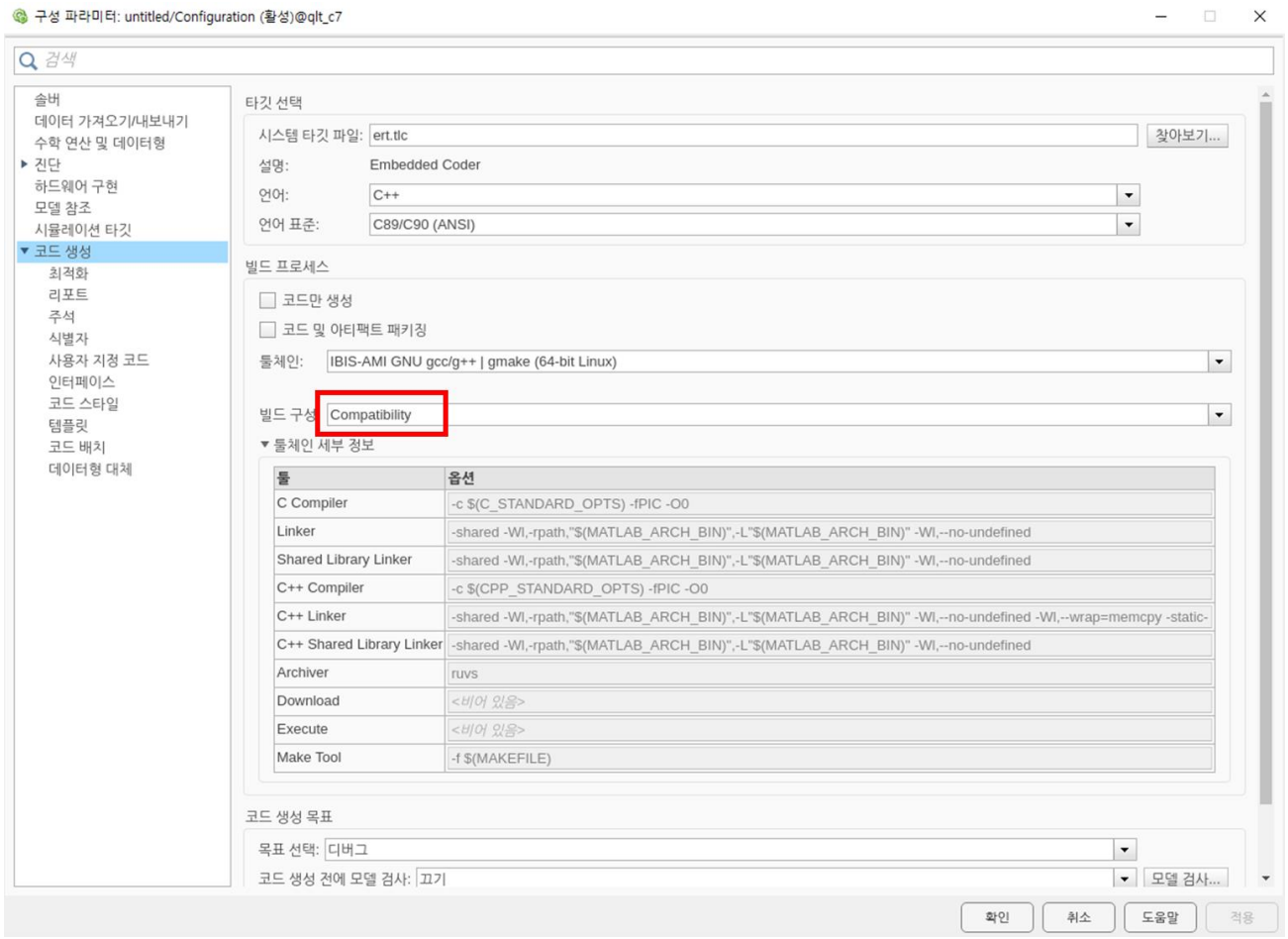
- SerDes IBIS-AMI Manager configurations
  - Export GetWave, Init, or Dual IBIS-AMI models



IBIS-AMI model generation (3/3)

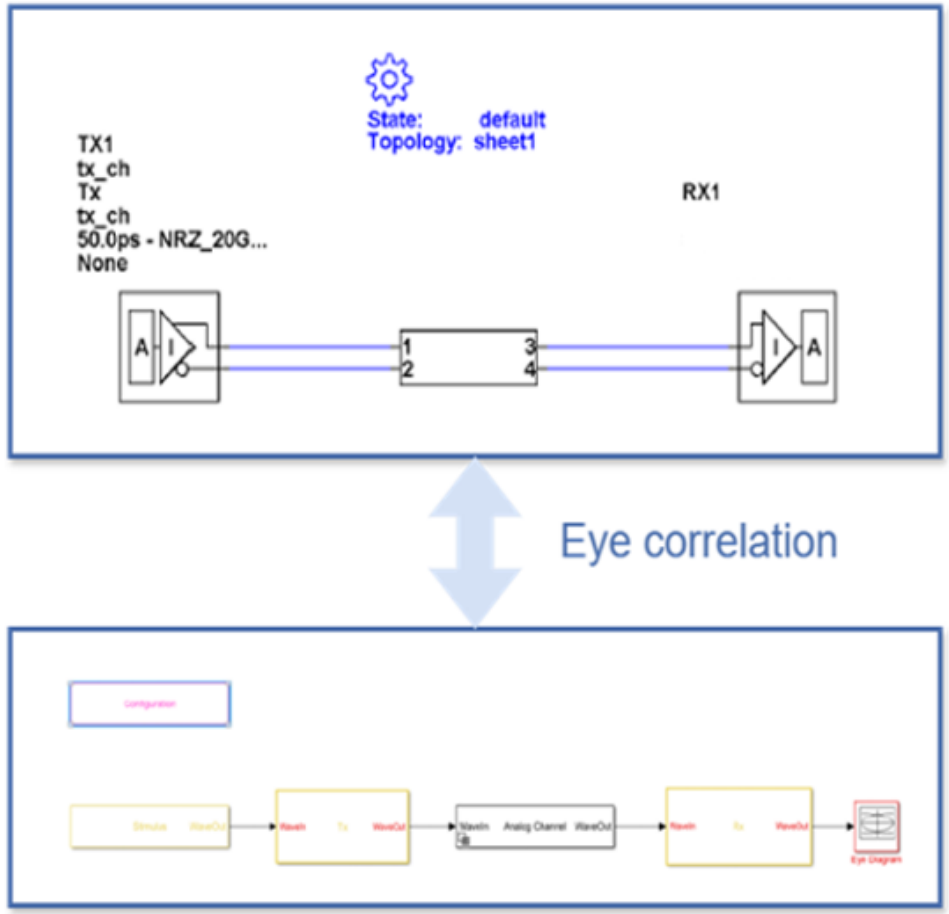
- Simulink Coder in MATLAB

  For Linux Compatibility,
  Simulink Coder is solution



IBIS-AMI model Verification (1/2)

- MATLAB SI toolbox simulation

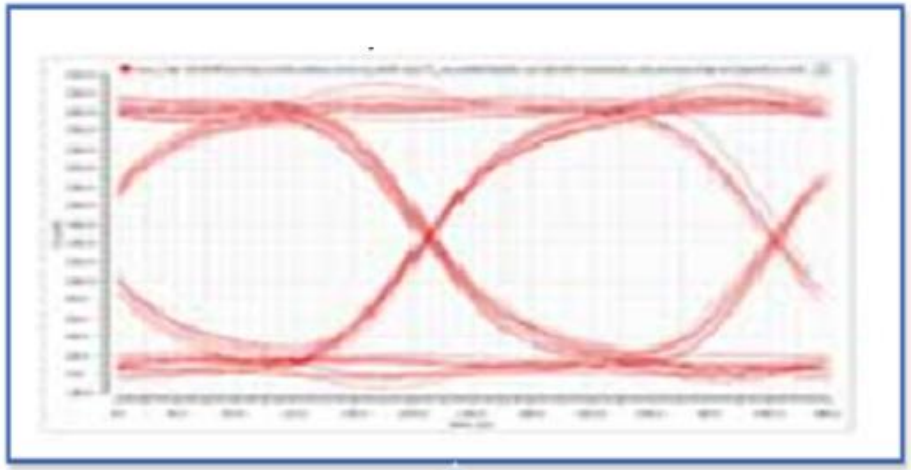


SI toolbox simulation

Simulink simulation

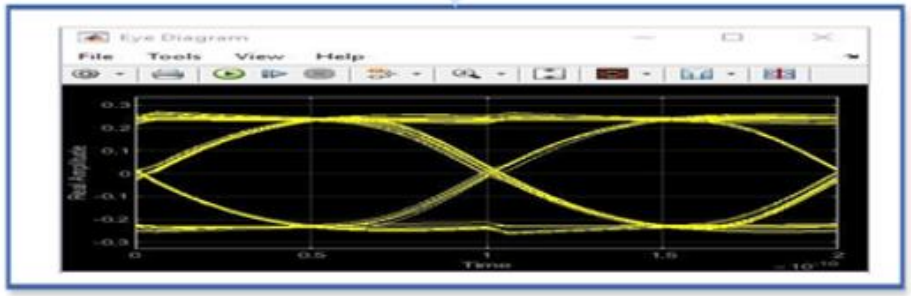
IBIS-AMI model Verification (2/2)

- Spice simulation



Spice simulation

Eye correlation



Simulink simulation

Contents

- Key takeaways
- IBIS & IBIS-AMI Overview
- IBIS-AMI model Generation and Compatibility
- MATLAB Toolboxes in IBIS-AMI Modeling
  - Model Generation in SerDes Toolbox
  - Model Verification in Simulink
- **Conclusions**

Key Outcomes/Advantages

- Reduced development time for the IBIS-AMI model by 30-40% using SerDes Toolbox
- Eliminated Linux compatibility issues, saving about 40% of time needed for model management
- Enable designers to collaborate more easily and effectively for Model-Based Design using Simulink

Installed Matlab and IBIS-AMI generation Server information

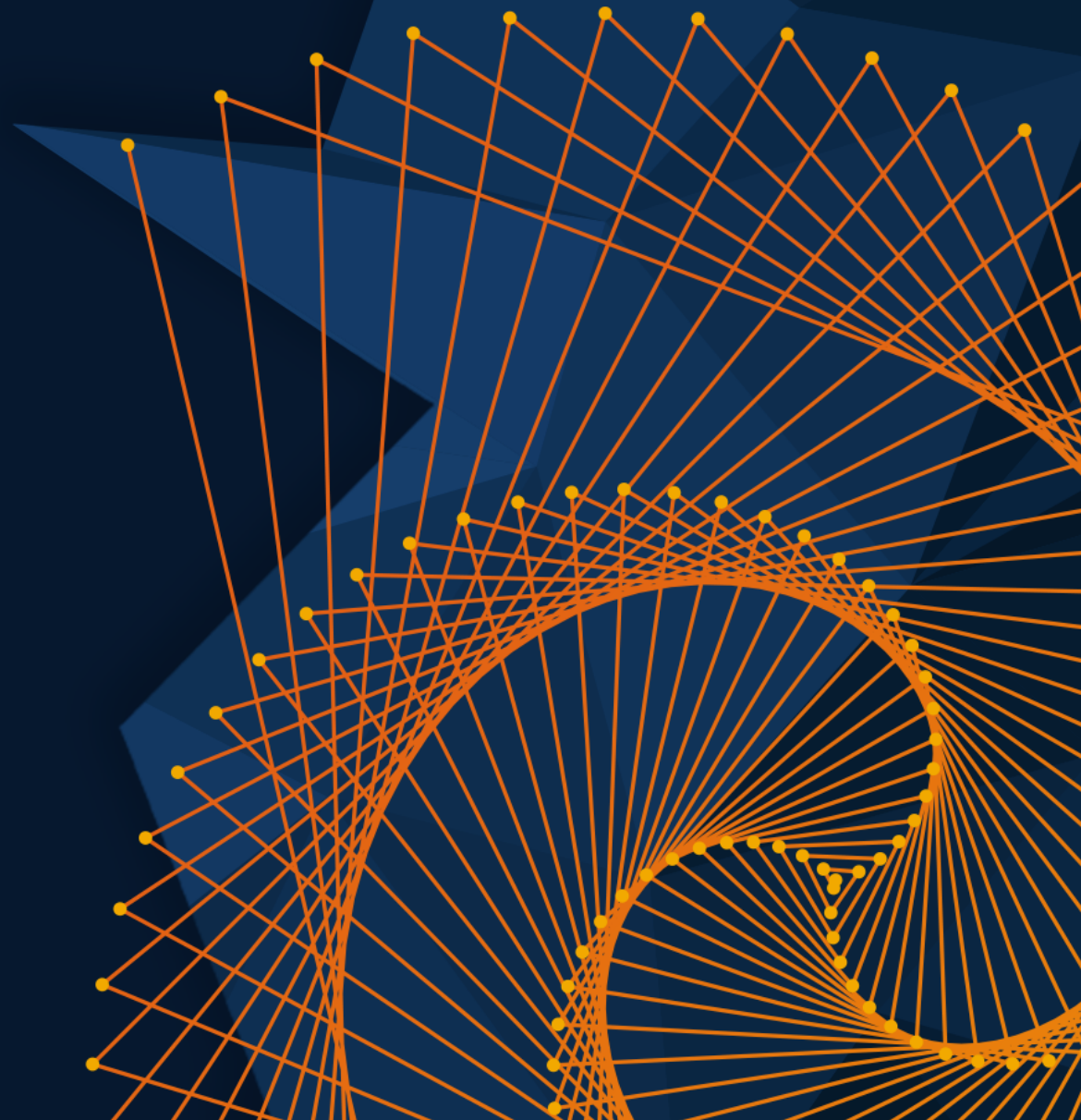
OS	GLIBC ver.	GLIBCXX ver.	CXXABI ver.	GCC ver.
CentOS 7.9.2009	2.17	3.4.19	1.3.7	4.8.5

IBIS-AMI verification Server information					Simulink Coder	IBIS-AMI verification Tool	IBIS-AMI verification Results
Server OS	**GLIBC ver.**	**GLIBCXX ver.**	**CXXABI ver.**	**GCC ver.**	**Before/After make -f Tx(Rx).mk**	**Hspice(Synopsys)**	**Error Log**
CentOS 7.9.2009	2.17	3.4.19	1.3.7	4.8.5	Before	O	-
	2.17	3.4.19	1.3.7	4.8.5	After	O	-
Redhat 7.9	2.17	3.4.19	1.3.7	4.8.5	Before	O	-
	2.17	3.4.19	1.3.7	4.8.5	After	O	-
CentOS 6.10	2.12	3.4.13	1.3.3	4.4.7	Before	X	**GLIBC_2.14 not found**
	2.12	3.4.13	1.3.3	4.4.7	After	O	-

Future Opportunities

- Accuracy vs. Speed → Optimal Accuracy
- Reflect silicon behavior across P.V.T
- Reduced regression using optimal methodology

MATLAB EXPO



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