



November 13–14, 2024 | Online

Integrated Development Workflow for 5G Applications Using AMD Versal™ Adaptive SoC

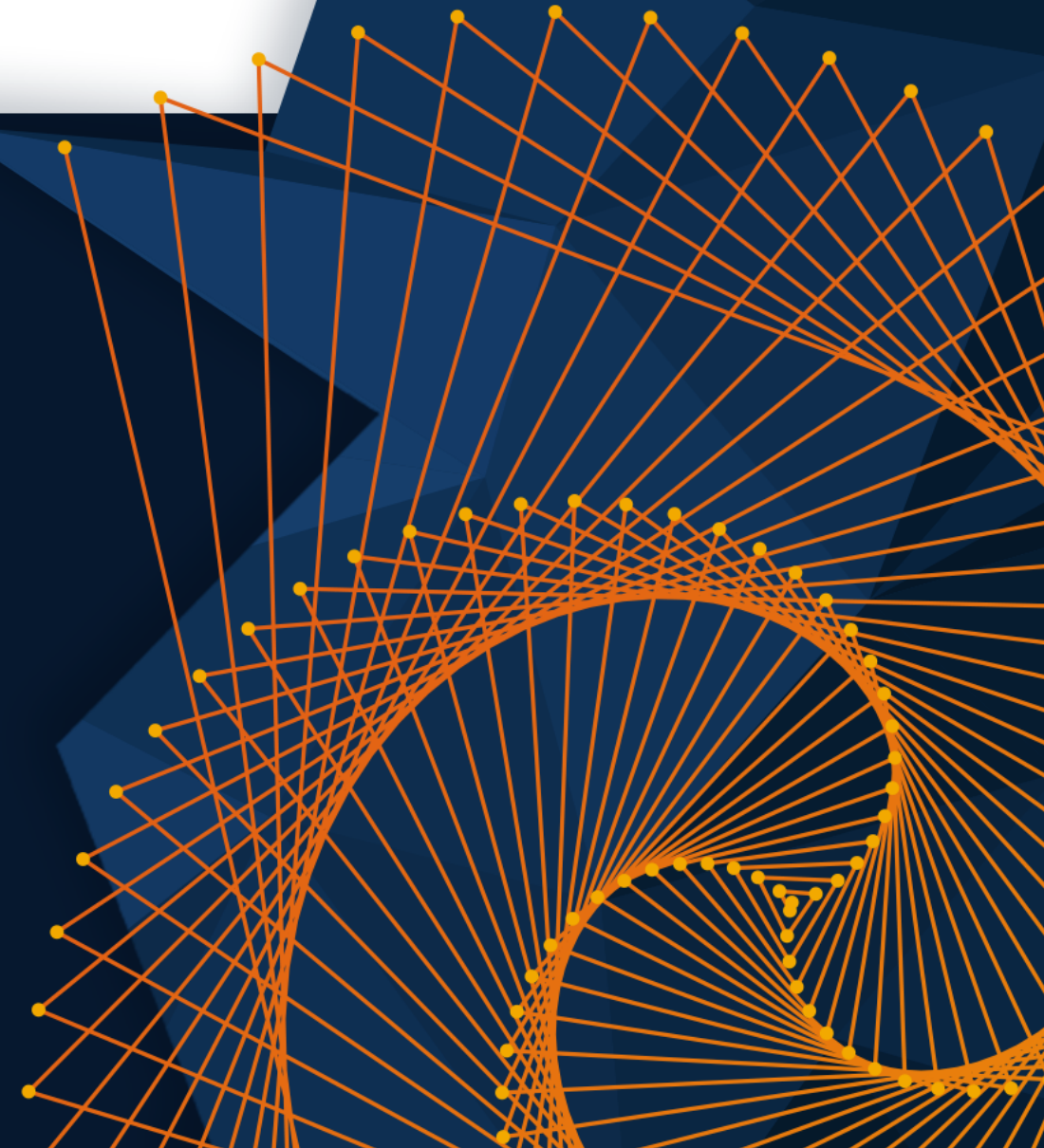
Rob Graessle, AMD



Noam Levine, MathWorks



MATLAB EXPO

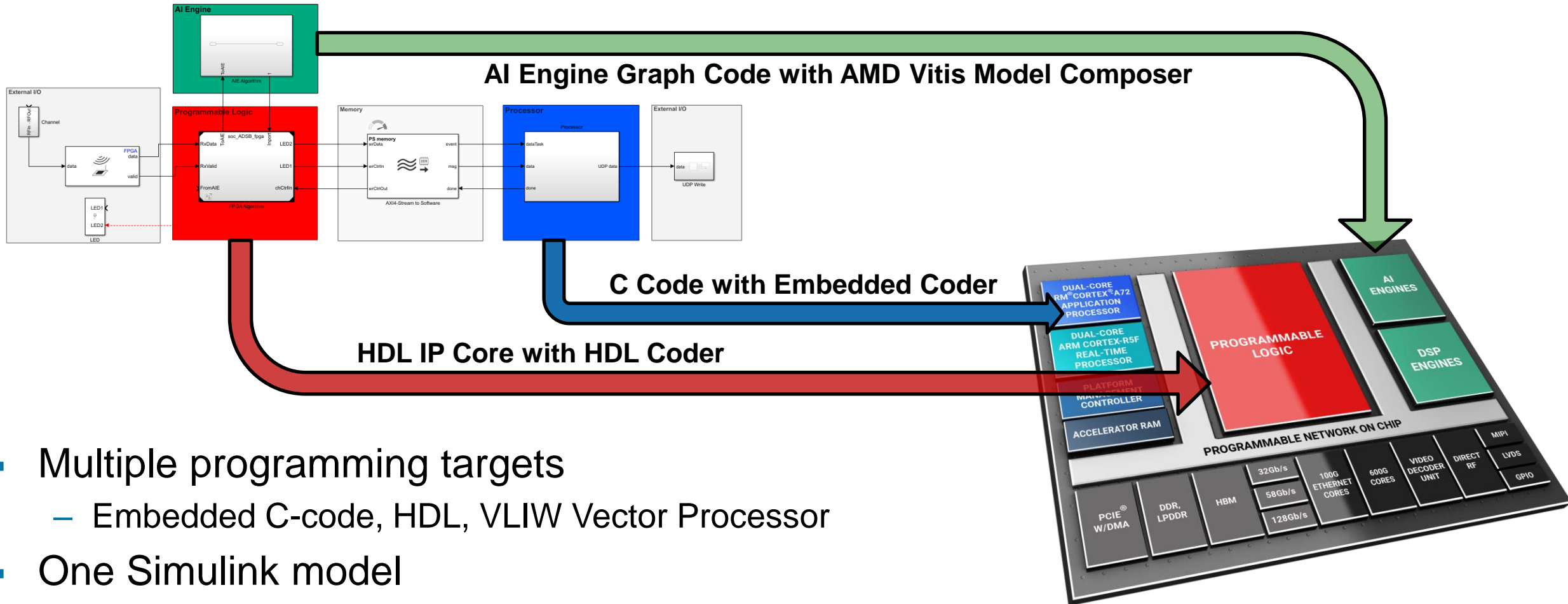


Agenda

- Workflow Overview
- AMD Versal Adaptive SoCs and AMD Vitis™ Model Composer
- Connecting HDL Coder from MathWorks to AMD Vitis Model Composer

Workflow Overview

Targeting all Versal Programmable Engines from MATLAB and Simulink



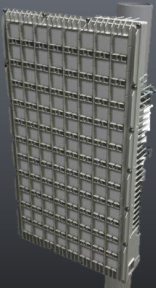
- Multiple programming targets
 - Embedded C-code, HDL, VLIW Vector Processor
- One Simulink model
 - Unified design and simulation environment

AMD Versal Adaptive SoCs and AMD Vitis Model Composer

AMD Versal™ Adaptive SoCs Everywhere

AMD 
VERSAL
AI Core

5G Beamforming



AMD 
VERSAL
AI Edge Gen 2

AI-Enabled
Stereo Camera



AMD 
VERSAL
HBM

8K Camera



AMD 
VERSAL
Premium

800G Test & Comms
Infrastructure

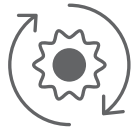


AMD 
VERSAL
Prime

Satellite-Based
Internet Services



AMD Versal™ Adaptive System-on-Chip



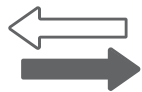
Processing System



Programmable Logic



AI Engines
SW Programmable, HW Adaptable



Breakout Integration of Advanced Protocol Engines



Network on Chip



Introduction to AMD Versal™ AI Engine

First introduced in AMD Versal™ AI Core Series

Software programmable

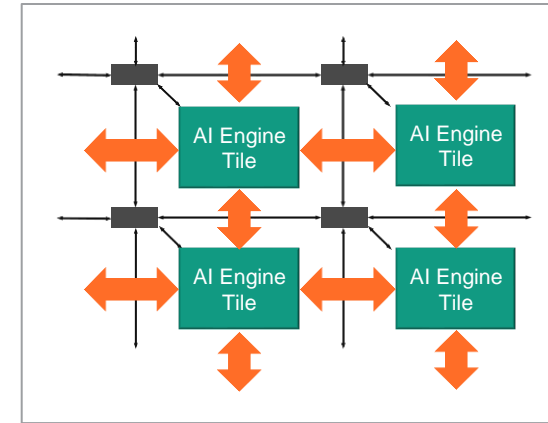
- VLIW processor running at 1 GHz+
- Massively reduce development time vs traditional RTL

Array of vector processors running at 1 GHz+

- From 8 tiles on the smallest device (VE2002)
- Up to 472 tiles on the largest device (VP2802)

Terabytes/sec of interface bandwidth

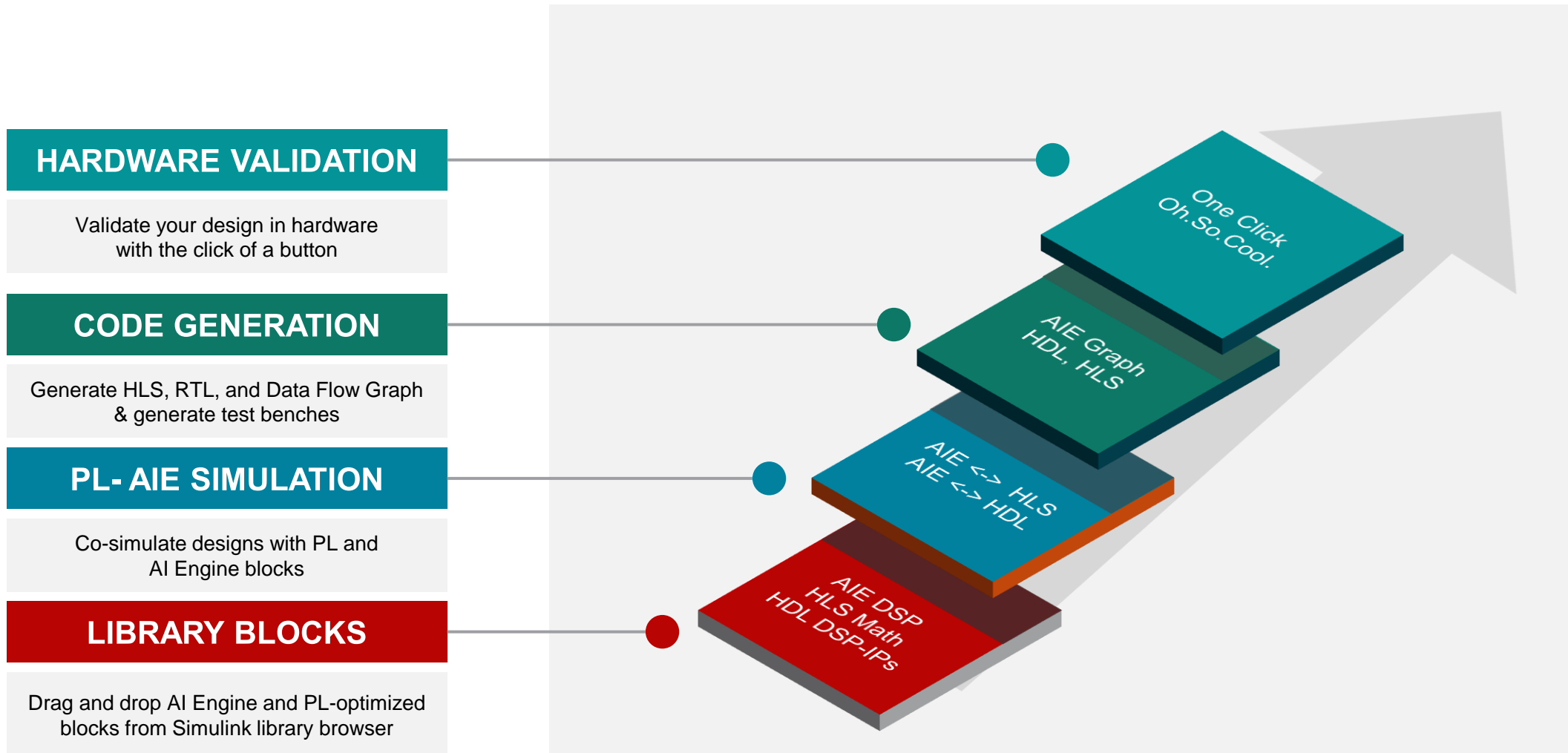
- Direct, massive throughput to adaptable hardware engines



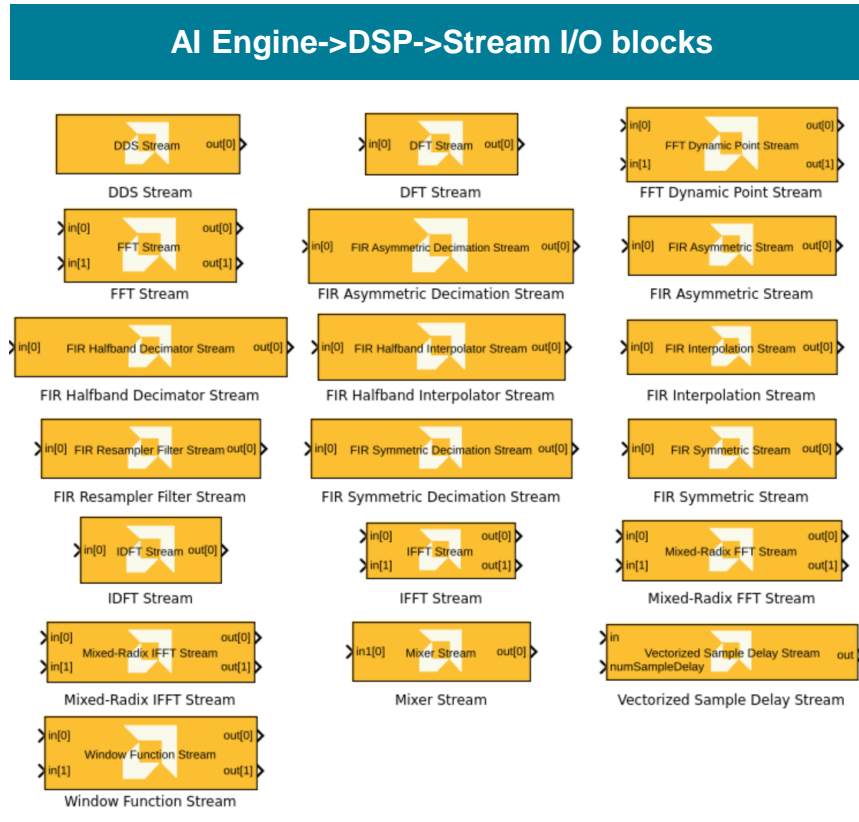
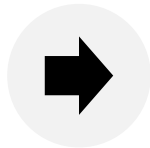
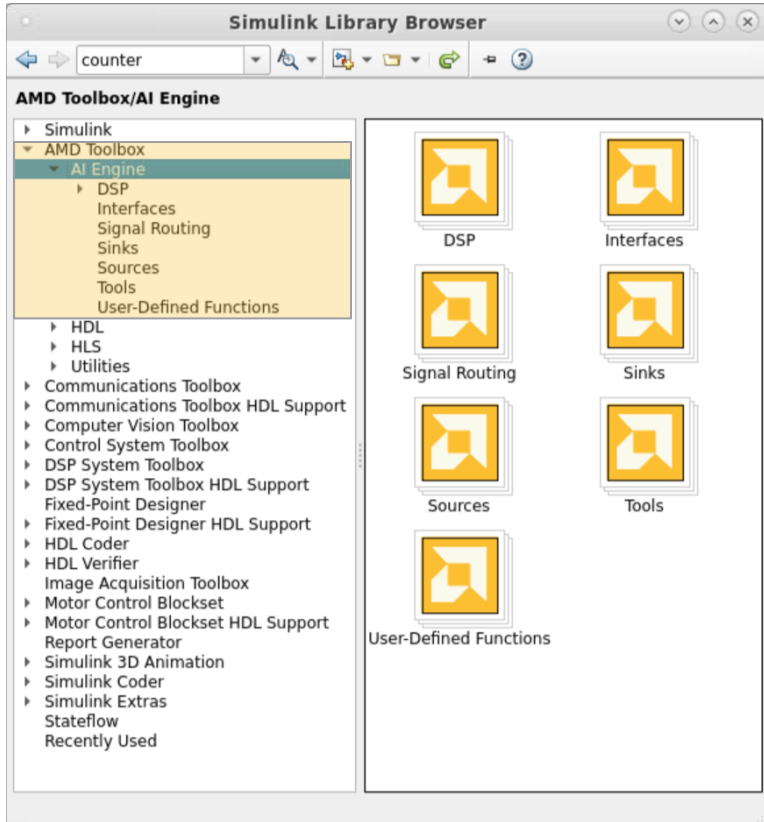
Integrated Workflow for AI Engine Development

AMD Vitis Model Composer **accelerates** Versal development by offering a **productive** environment within MathWorks Simulink® for **simulation, code generation,** and **hardware validation.**

AMD Vitis™ Model Composer At A Glance



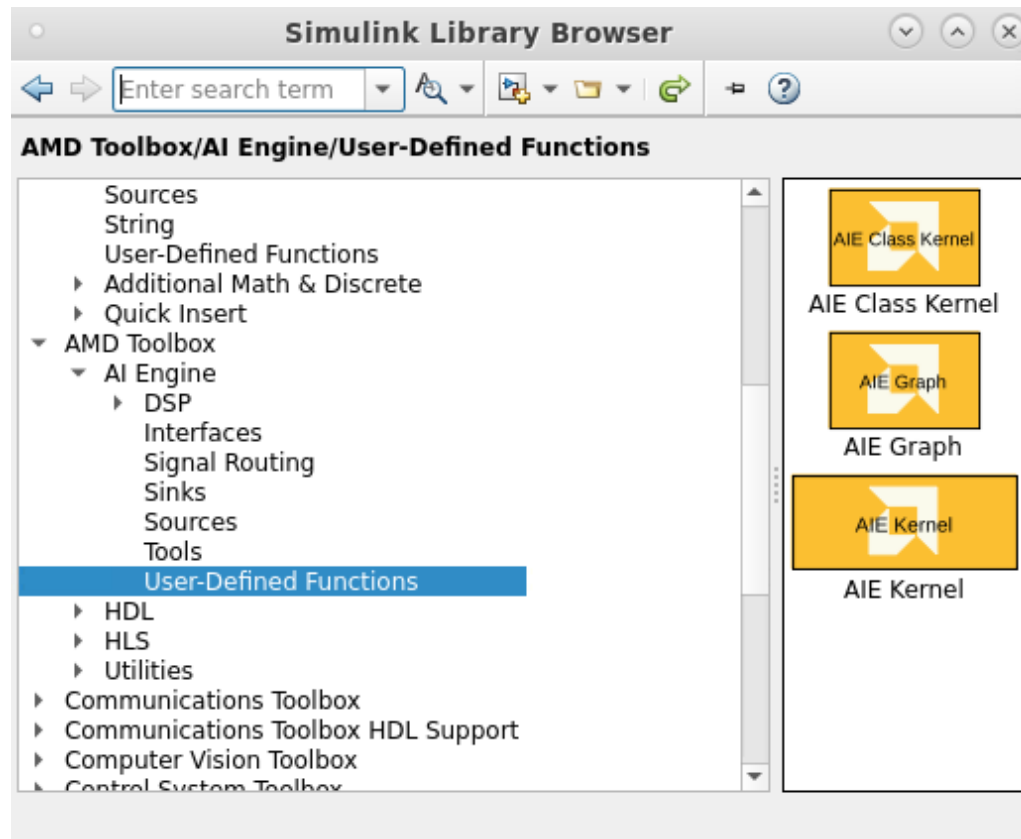
AI Engine Library Blocks



Bit accurate

AIE and AIE-ML devices

Import Custom AI Engine Code as a Block



Import code :

*.cpp

*.cc

*.h

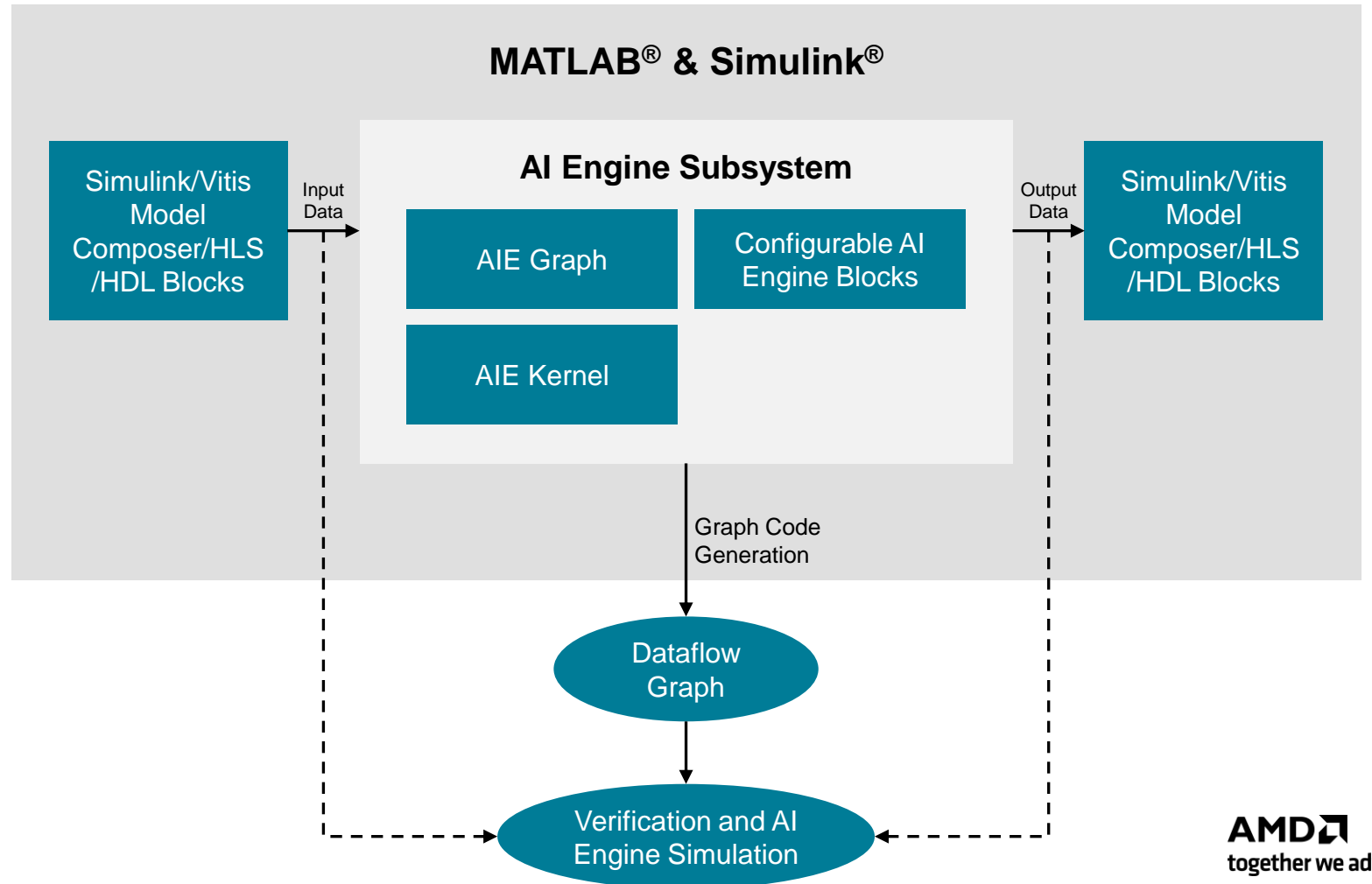
...and connect to other blocks

AMD Vitis™ Model Composer for AIE Development

AMD Vitis™ Model Composer is a model-based design tool that enables rapid design exploration within the MathWorks MATLAB® and Simulink® environment.

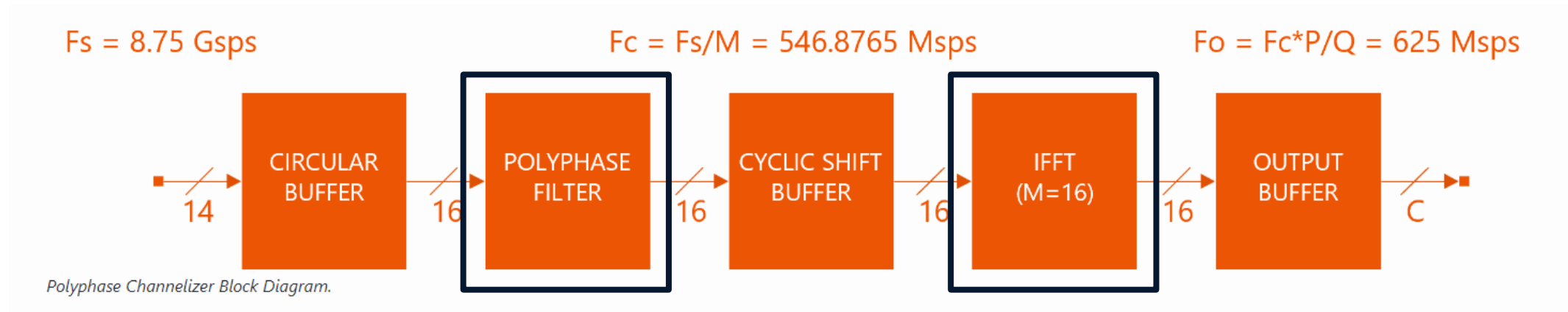
Advantages for AIE-DSP Design Flow:

- **Automatically generate Graph C Code for AI Engines**
- **Import HDL blocks in AIE designs**
- **Heterogeneous simulation with robust test bench capabilities from Simulink®**



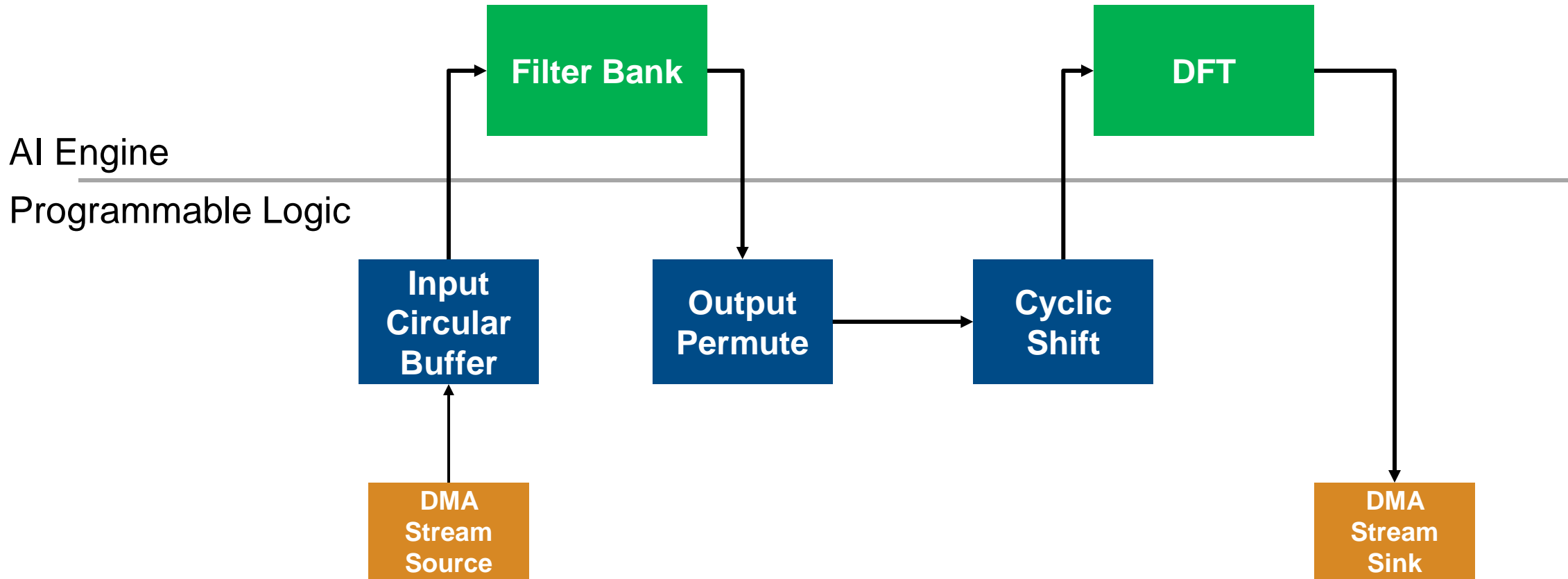
Connecting HDL Coder from MathWorks to AMD Vitis Model Composer

Example – Polyphase Channelizer

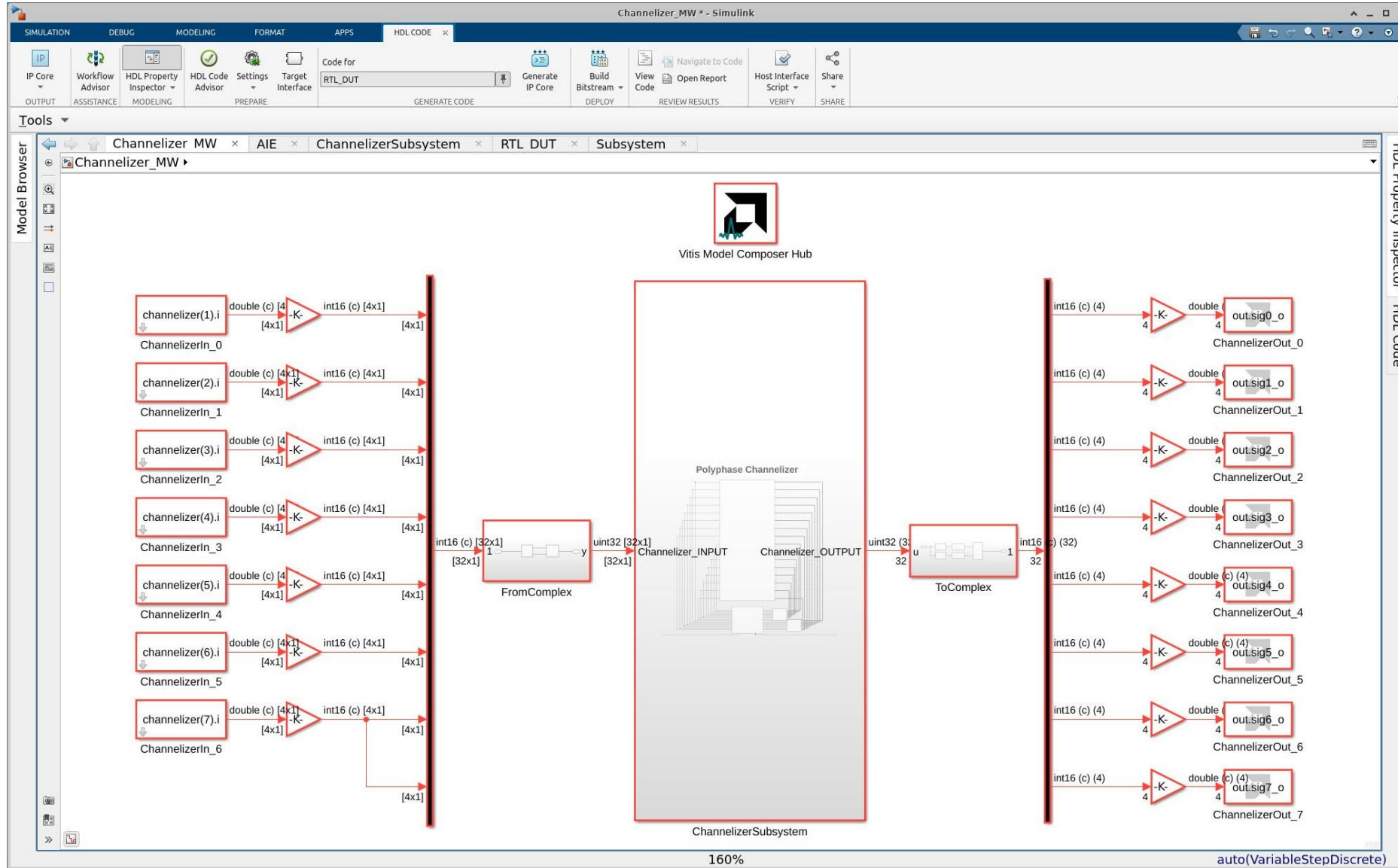


From https://github.com/Xilinx/Vitis_Model_Composer/tree/2024.1/Examples/AIENGINE_plus_PL/AIE_HLS/Channelizer

System Partitioning



Top-Level Simulink Implementation



Simulink Implementation

The screenshot displays the Simulink HDL Code editor for a project named "Channelizer_MW/ChannelizerSubsystem". The main workspace shows a block diagram titled "Polyphase Channelizer". The diagram consists of several parallel processing paths, each starting with a "FromCyclicDNR" block followed by a "ToOutputPermuse" block. The paths are labeled "FromCyclicDNR_0" through "FromCyclicDNR_7" and "ToOutputPermuse_0" through "ToOutputPermuse_7".

Four large orange arrows are overlaid on the diagram, numbered 1 through 4:

- Arrow 1 points to the input side of the parallel paths.
- Arrow 2 points to the output side of the parallel paths.
- Arrow 3 points to the "AIE Target" block, which is a central processing unit.
- Arrow 4 points to the output side of the "AIE Target" block.

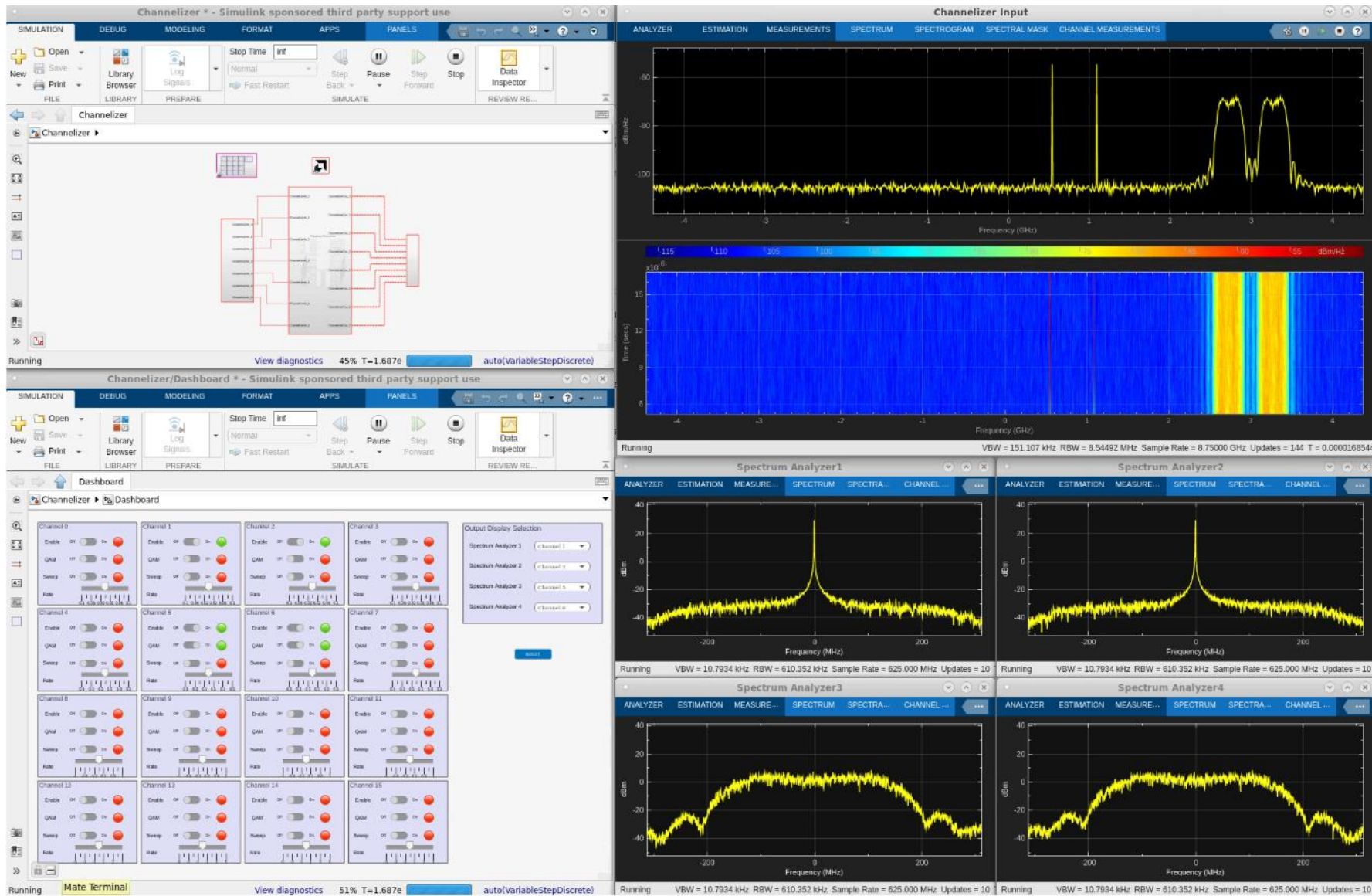
A black arrow labeled "PL Target" points from the text "PL Target" to the "AIE Target" block. Below the main diagram, there is a detailed view of the "AIE Target" block, showing its internal structure with various signal paths and components.

At the bottom of the window, there are two data flow indicators:

- "From MATLAB workspace" with an arrow pointing to a "Channelizer_INPUT" block.
- "To MATLAB workspace" with an arrow pointing from a "Channelizer_OUTPUT" block.

The status bar at the bottom indicates "70%" completion and "auto(VariableStepDiscrete)".

Model Simulation



Environment Setup for Deployment

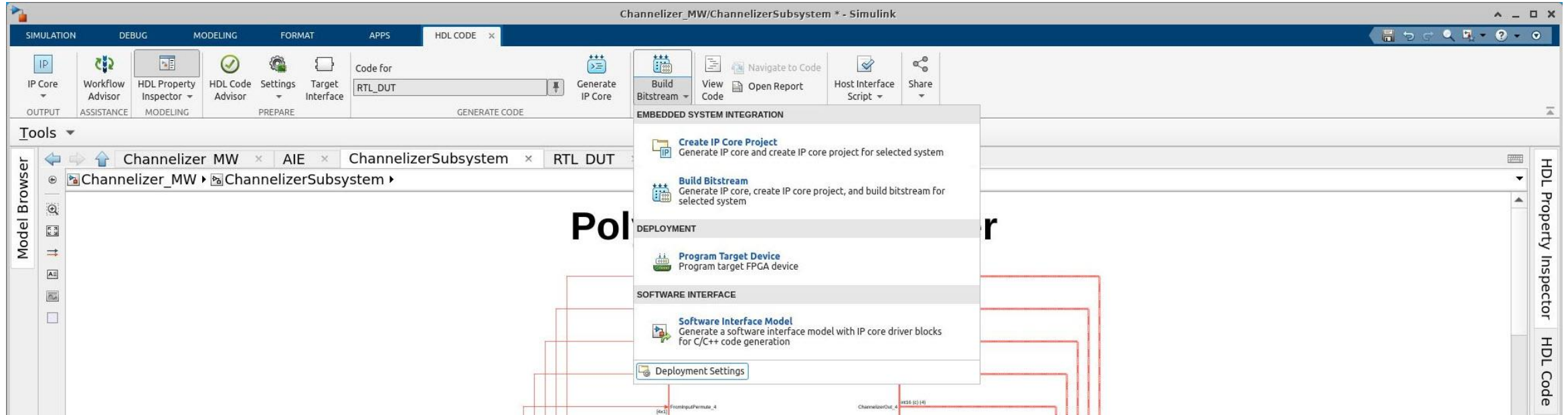
The screenshot displays the HDL Code Editor for a Simulink model named 'Channelizer_MW'. The main workspace shows a block diagram of the 'ChannelizerSubsystem' with various input and output blocks. The 'IP Core - Channelizer_MW/Channelizer/RTL_DUT' configuration window is open, showing the 'Interface Mapping' tab. This window includes a table defining the mapping between source ports and target interfaces.

Source	Port Type	Data Type	Interface	Interface Mapping
FB1Out	Inport	int16 (c)...	AI Engine FilterBank1 Slave	Data
FB2Out	Inport	int16 (c)...	AI Engine FilterBank2 Slave	Data
FB3Out	Inport	int16 (c)...	AI Engine FilterBank3 Slave	Data
FB4Out	Inport	int16 (c)...	AI Engine FilterBank4 Slave	Data
FB5Out	Inport	int16 (c)...	AI Engine FilterBank5 Slave	Data
FB6Out	Inport	int16 (c)...	AI Engine FilterBank6 Slave	Data
FB7Out	Inport	int16 (c)...	AI Engine FilterBank7 Slave	Data
FB8Out	Inport	int16 (c)...	AI Engine FilterBank8 Slave	Data
ChannelizerIn_0	Inport	int16 (c)...	AI Engine DFT1 Slave	Data
ChannelizerIn_1	Inport	int16 (c)...	AI Engine DFT2 Slave	Data
ChannelizerIn_2	Inport	int16 (c)...	AI Engine DFT3 Slave	Data
ChannelizerIn_3	Inport	int16 (c)...	AI Engine DFT4 Slave	Data
ChannelizerIn_4	Inport	int16 (c)...	AI Engine DFT5 Slave	Data

- Define I/O ports for blocks targeted to Programmable Logic and AI Engine
- Blocks targeted to Programmable Logic will go through HDL Coder
- Blocks targeted to AI Engines will go through AMD Vitis Model Composer

New Workflow Access from the Simulink Desktop

- Access to HDL Coder workflows now available in the Simulink Toolstrip



Summary

- AMD Versal Adaptive SoCs provide a heterogeneous compute environment combining processor cores and programmable logic with a powerful VLIW vector processing “AI Engine” to speed signal processing calculations
- Using HDL Coder from MathWorks *with* AMD Vitis Model Composer enables users to target all the programmable engines on Versal from a single Model-Based Design environment

For More Information

1. Visit **MathWorks.com/AMD** for more information on targeting workflows for AMD Adaptive FPGAs and SoCs
2. Contact **fpga_expert@mathworks.com** if you want to evaluate this workflow using HDL Coder with AMD Vitis Model Composer

MATLAB EXPO



© 2024 The MathWorks, Inc. MATLAB and Simulink are registered trademarks of The MathWorks, Inc. See [mathworks.com/trademarks](https://www.mathworks.com/trademarks) for a list of additional trademarks. Other product or brand names may be trademarks or registered trademarks of their respective holders.

