November 13–14, 2024 | Online

Integrated Development Workflow for 5G Applications Using AMD Versal™ Adaptive SoC

Rob Graessle, AMD

Noam Levine, MathWorks

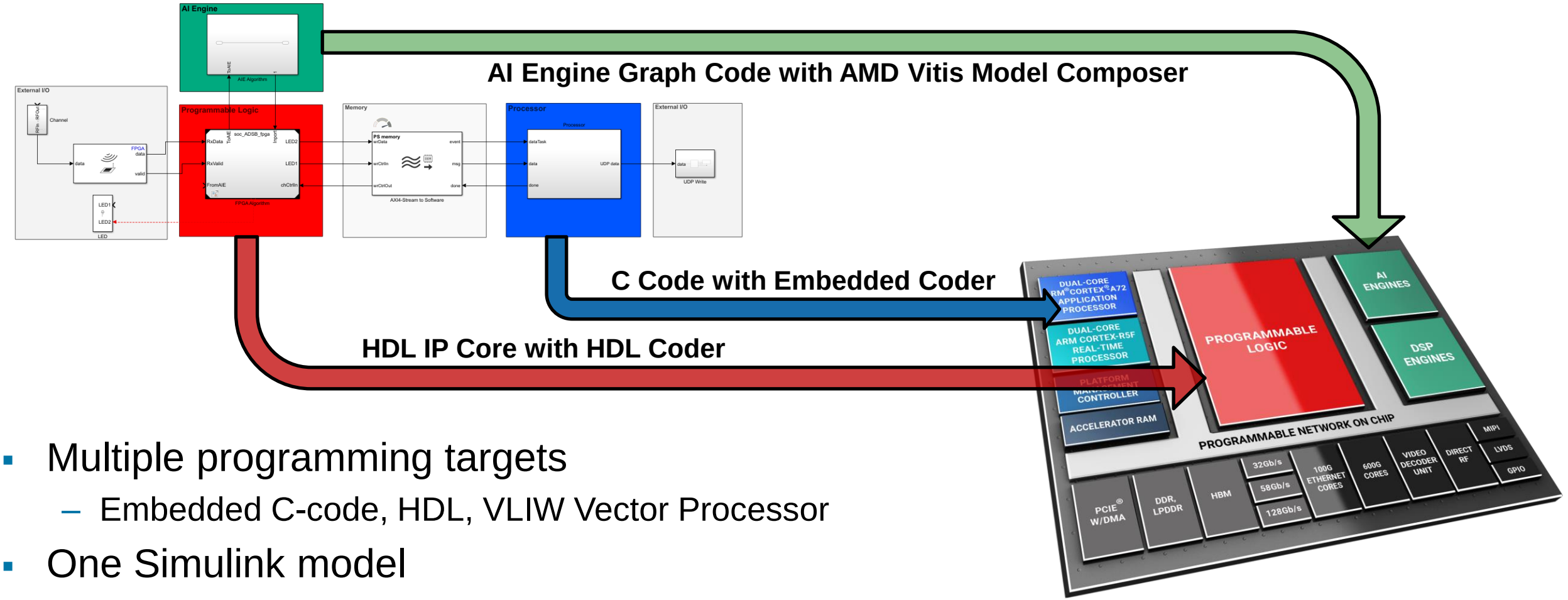
MATLAB EXPO

Agenda

- Workflow Overview
- AMD Versal Adaptive SoCs and AMD Vitis™ Model Composer
- Connecting HDL Coder from MathWorks to AMD Vitis Model Composer

Workflow Overview

Targeting all Versal Programmable Engines from MATLAB and Simulink



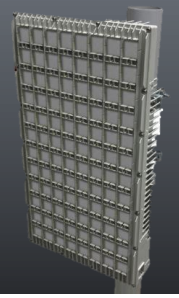
- Multiple programming targets
  - Embedded C-code, HDL, VLIW Vector Processor
- One Simulink model
  - Unified design and simulation environment

AMD Versal Adaptive SoCs
and
AMD Vitis Model Composer

AMD Versal™ Adaptive SoCs Everywhere

AMD VERSAL AI Core

5G Beamforming



AMD VERSAL AI Edge Gen 2

AI-Enabled Stereo Camera

AMD VERSAL HBM

8K Camera

AMD VERSAL Premium

800G Test & Comms Infrastructure

AMD VERSAL Prime

Satellite-Based Internet Services

AMD Versal™ Adaptive System-on-Chip

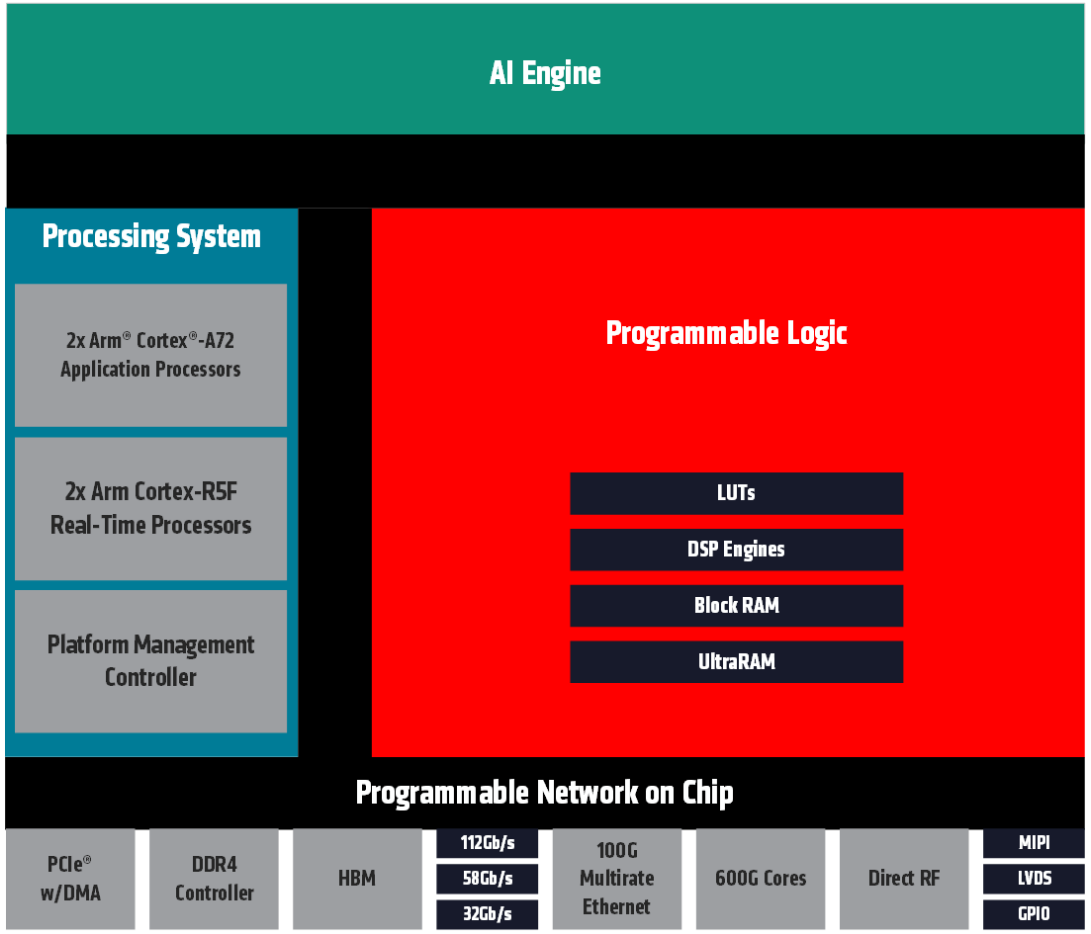
Processing System

Programmable Logic

AI Engines
SW Programmable, HW Adaptable

Breakout Integration of Advanced Protocol Engines

Network **o**n **C**hip



Introduction to AMD Versal™ AI Engine

First introduced in AMD Versal™ AI Core Series

Software programmable

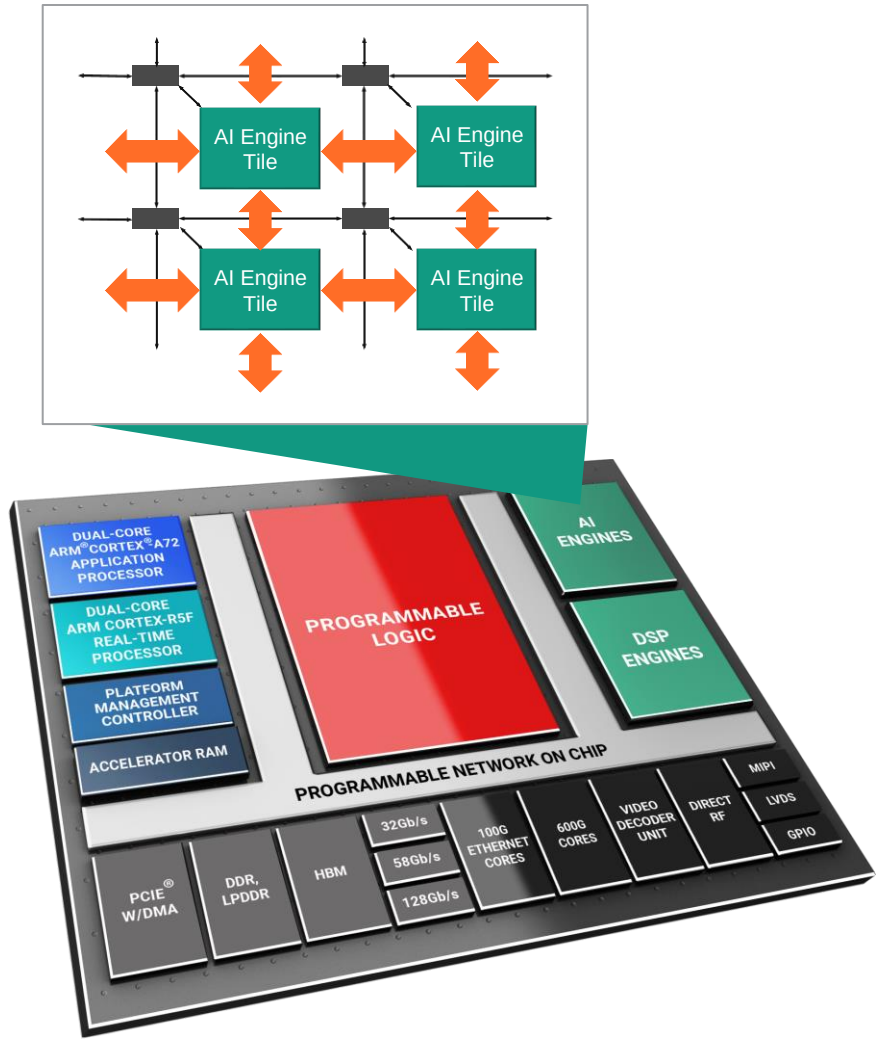
- VLIW processor running at 1 GHz+
- Massively reduce development time vs traditional RTL

Array of vector processors running at 1 GHz+

- From 8 tiles on the smallest device (VE2002)
- Up to 472 tiles on the largest device (VP2802)

Terabytes/sec of interface bandwidth

- Direct, massive throughput to adaptable hardware engines



Integrated Workflow for AI Engine Development

AMD Vitis Model Composer **accelerates** Versal development by offering a **productive** environment within MathWorks Simulink® for **simulation**, **code generation**, and **hardware validation**.

AMD Vitis™ Model Composer At A Glance

HARDWARE VALIDATION

Validate your design in hardware with the click of a button

CODE GENERATION

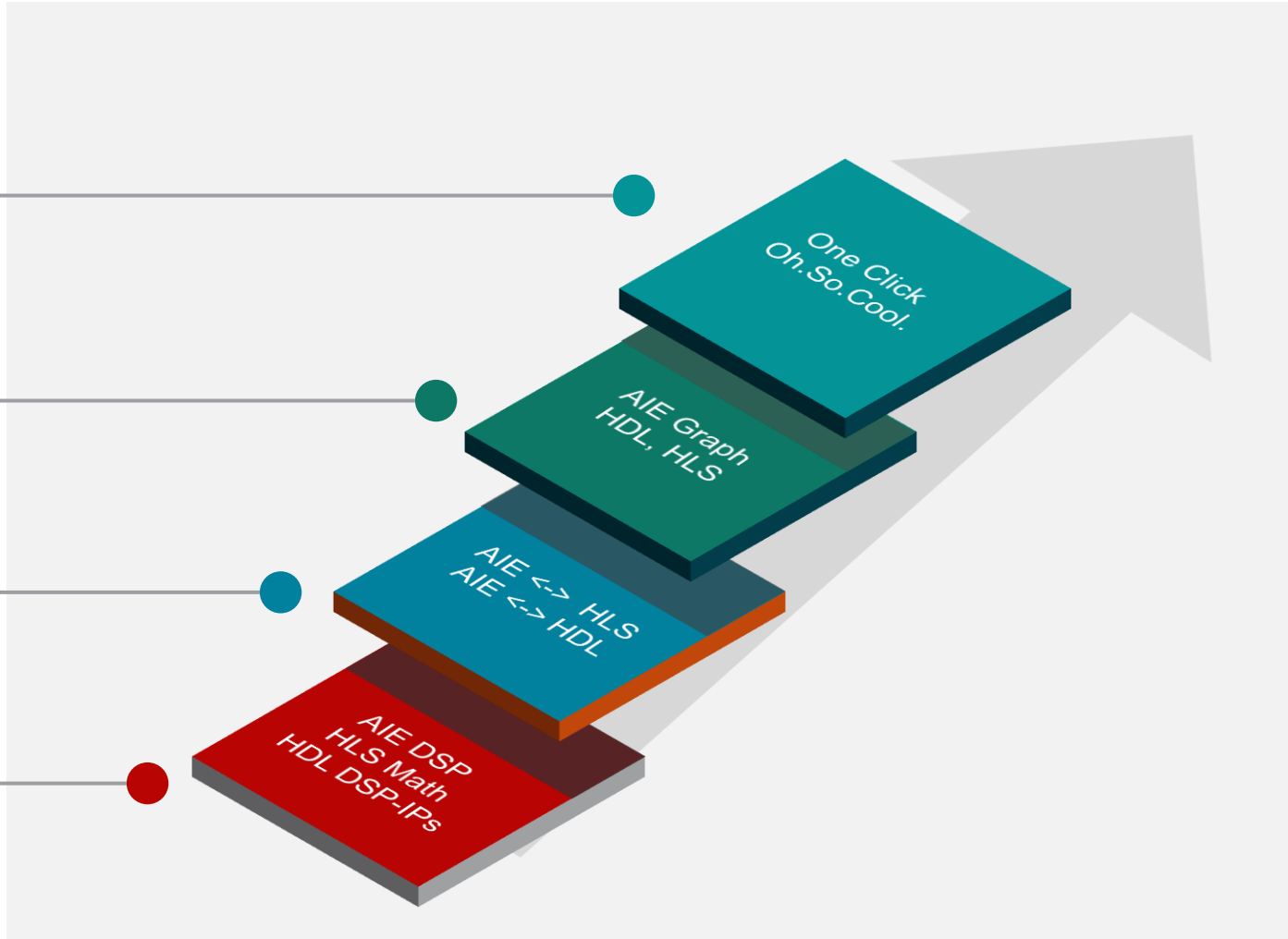
Generate HLS, RTL, and Data Flow Graph & generate test benches

PL- AIE SIMULATION

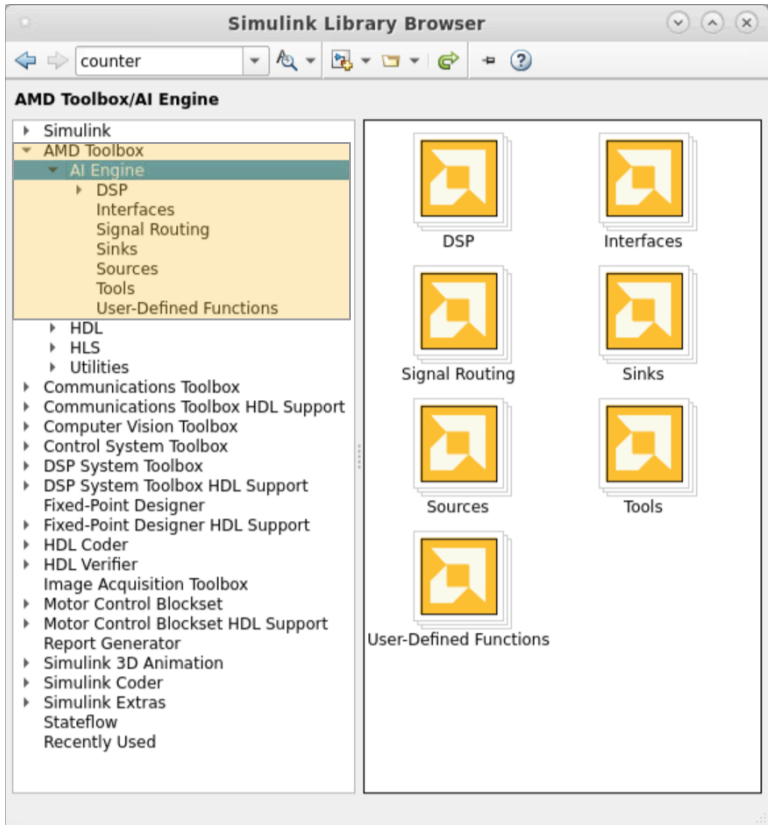
Co-simulate designs with PL and AI Engine blocks

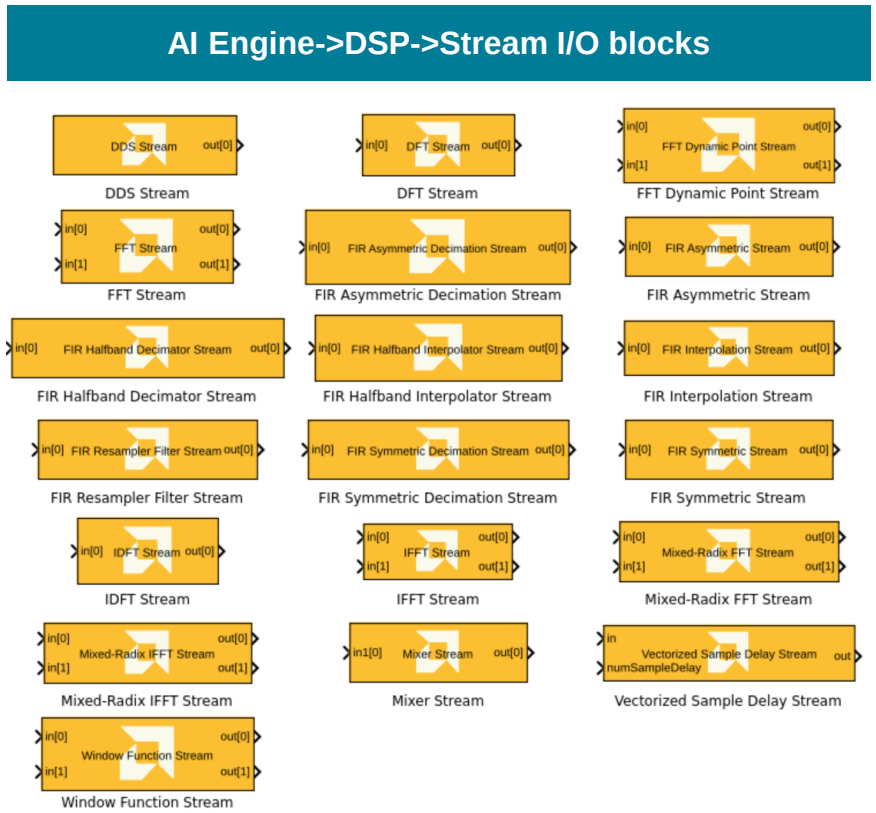
LIBRARY BLOCKS

Drag and drop AI Engine and PL-optimized blocks from Simulink library browser



AI Engine Library Blocks

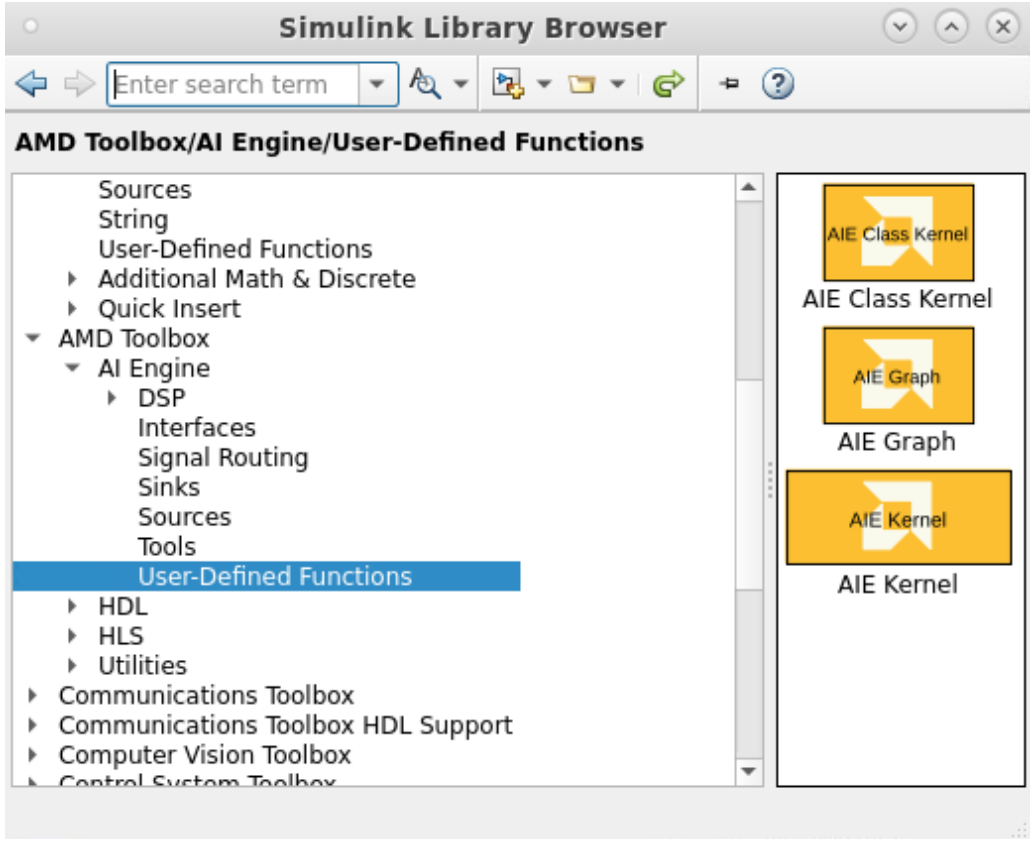




Bit accurate

AIE and AIE-ML devices

Import Custom AI Engine Code as a Block



Import code :

*.cpp

*.cc

*.h

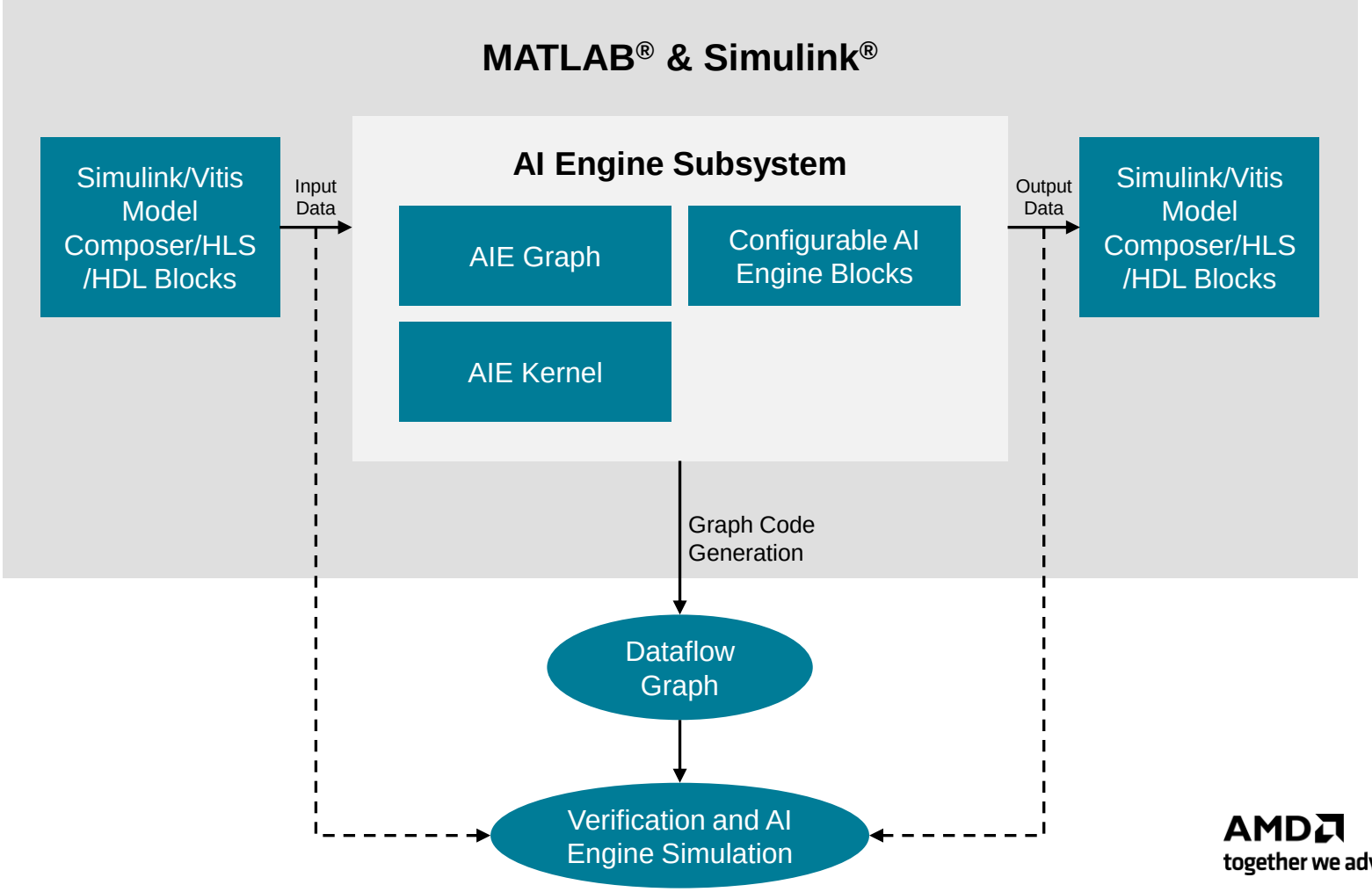
…and connect to other blocks

AMD Vitis™ Model Composer for AIE Development

AMD Vitis™ Model Composer is a model-based design tool that enables rapid design exploration within the MathWorks MATLAB® and Simulink® environment.

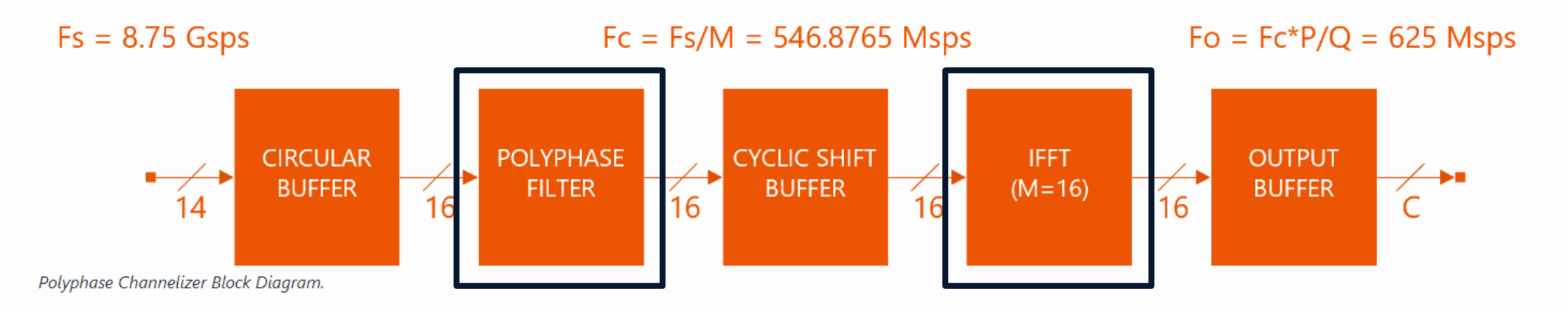
Advantages for AIE-DSP Design Flow:

- **Automatically generate Graph C Code for AI Engines**
- **Import HDL blocks in AIE designs**
- **Heterogeneous simulation with robust test bench capabilities from Simulink®**



Connecting HDL Coder from MathWorks to AMD Vitis Model Composer

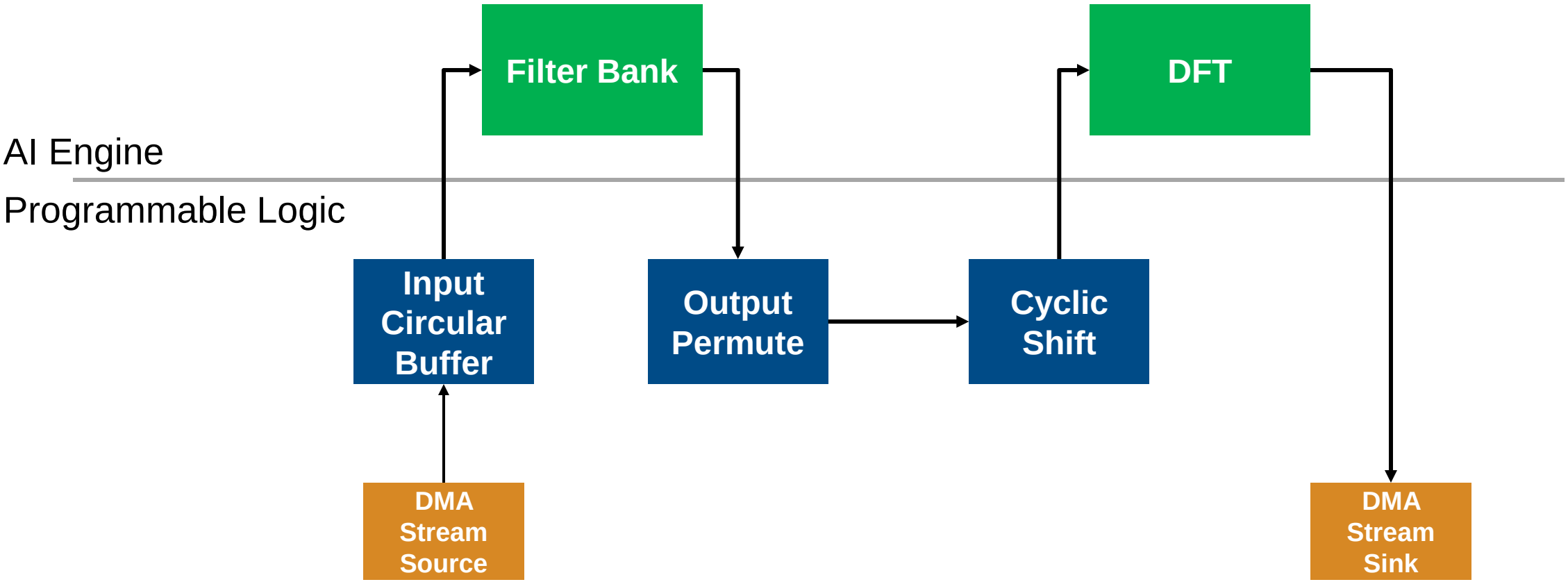
Example – Polyphase Channelizer



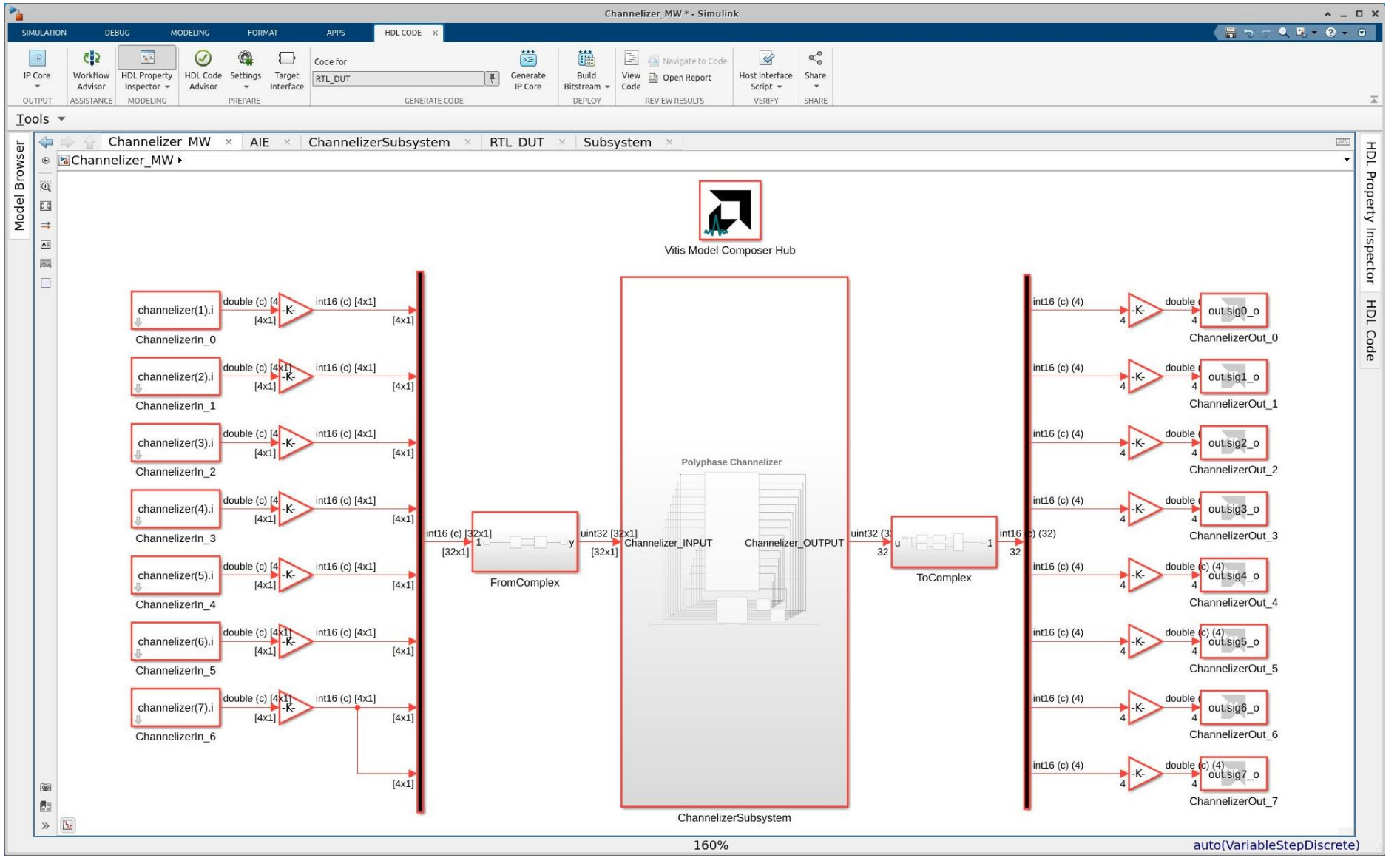
Polyphase Channelizer Block Diagram.

From https://github.com/Xilinx/Vitis_Model_Composer/tree/2024.1/Examples/AIENGINE_plus_PL/AIE_HLS/Channelizer

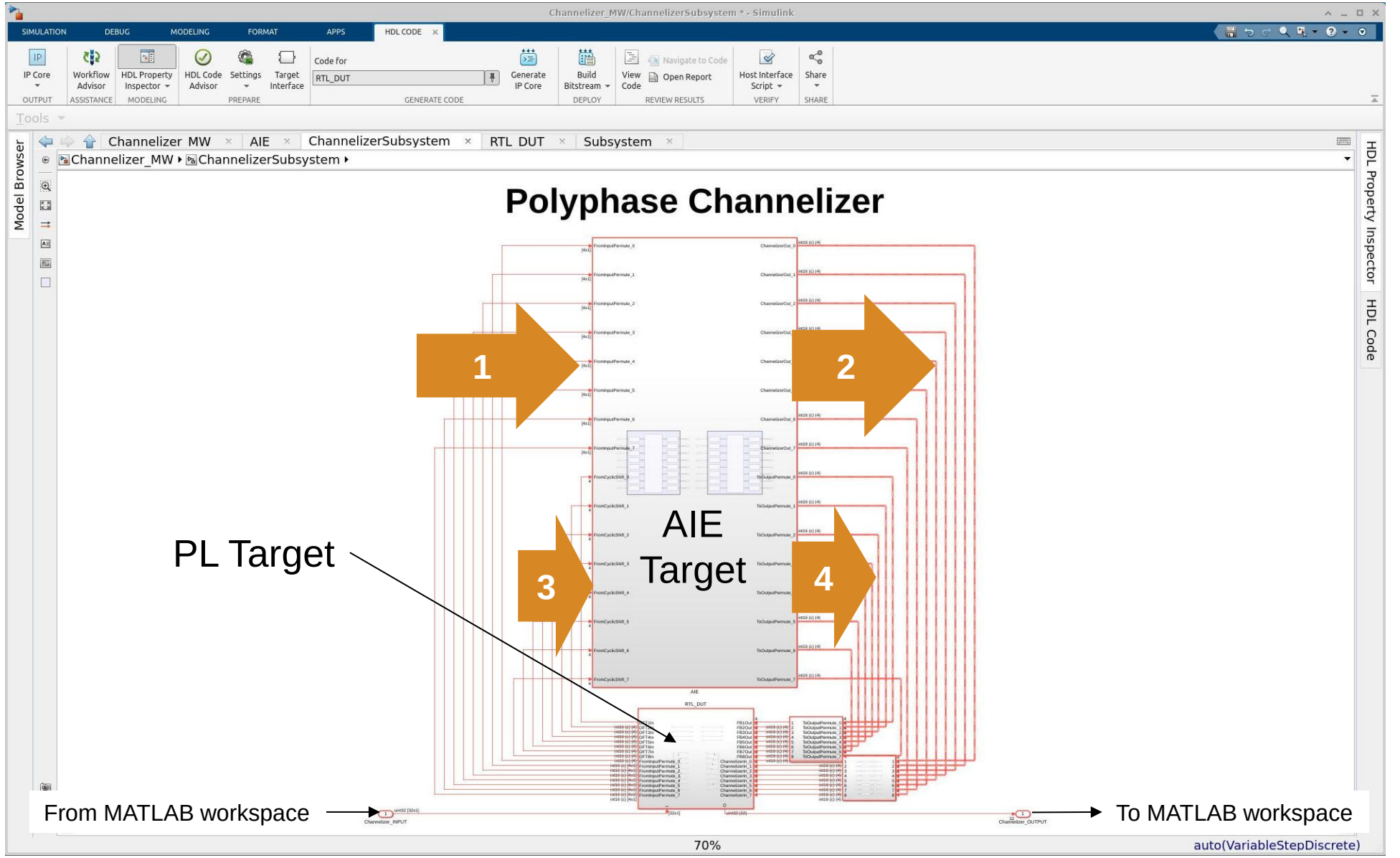
System Partitioning



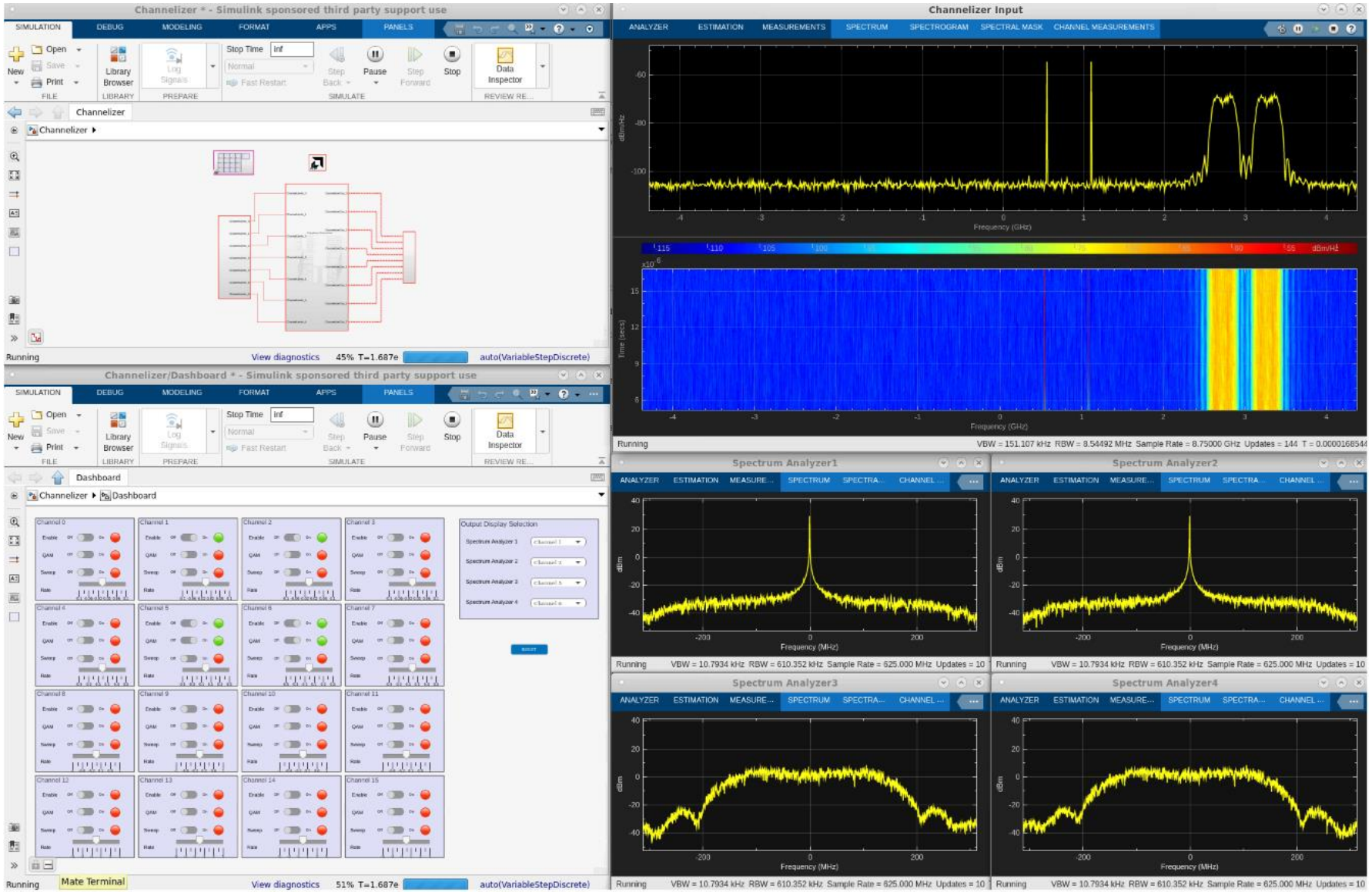
Top-Level Simulink Implementation



Simulink Implementation

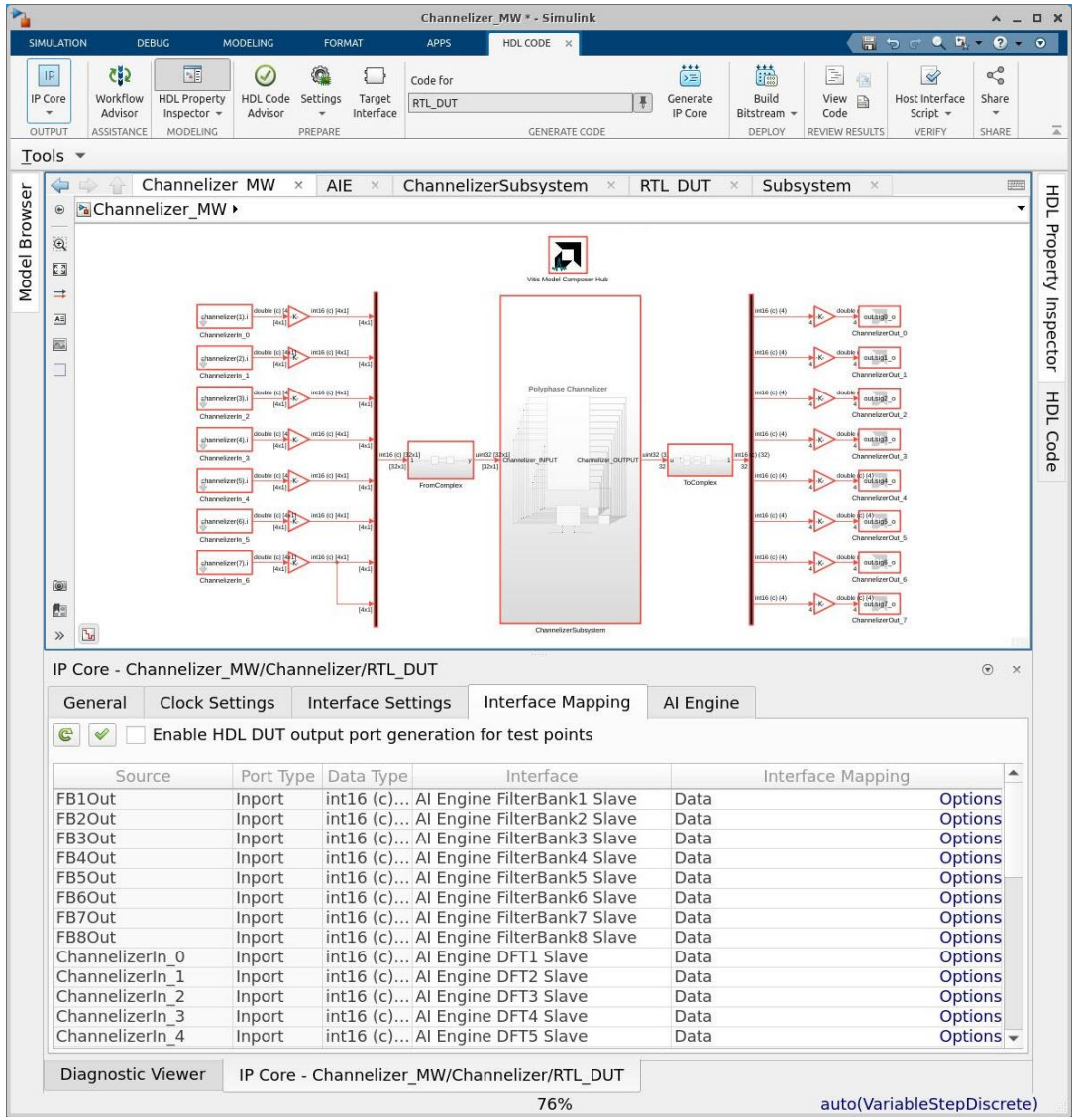


Model Simulation



MATLAB EXPO

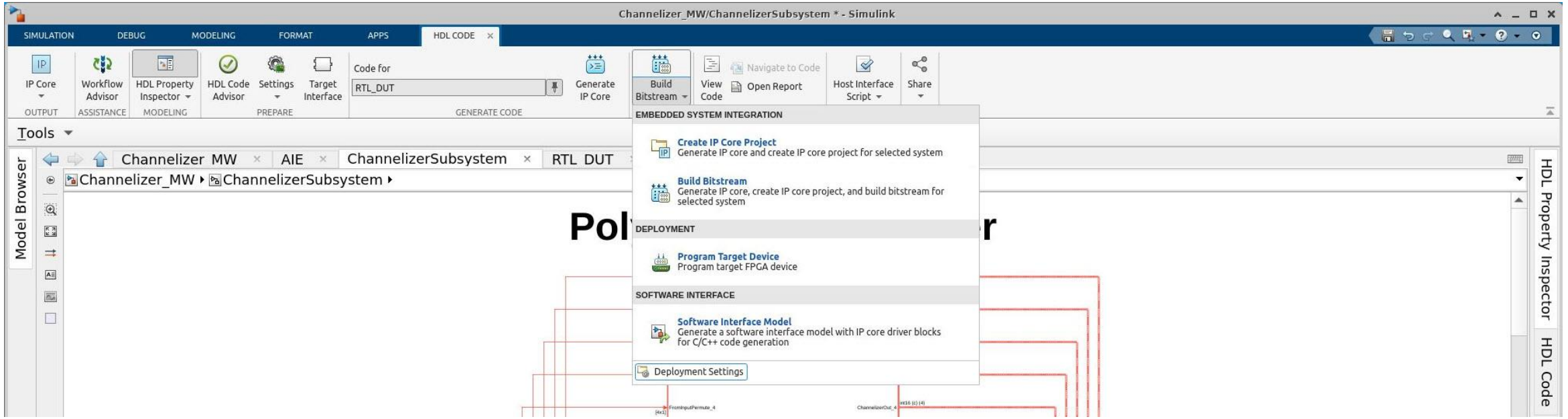
Environment Setup for Deployment



- Define I/O ports for blocks targeted to Programmable Logic and AI Engine
- Blocks targeted to Programmable Logic will go through HDL Coder
- Blocks targeted to AI Engines will go through AMD Vitis Model Composer

New Workflow Access from the Simulink Desktop

- Access to HDL Coder workflows now available in the Simulink Toolstrip



Summary

- AMD Versal Adaptive SoCs provide a heterogeneous compute environment combining processor cores and programmable logic with a powerful VLIW vector processing “AI Engine” to speed signal processing calculations

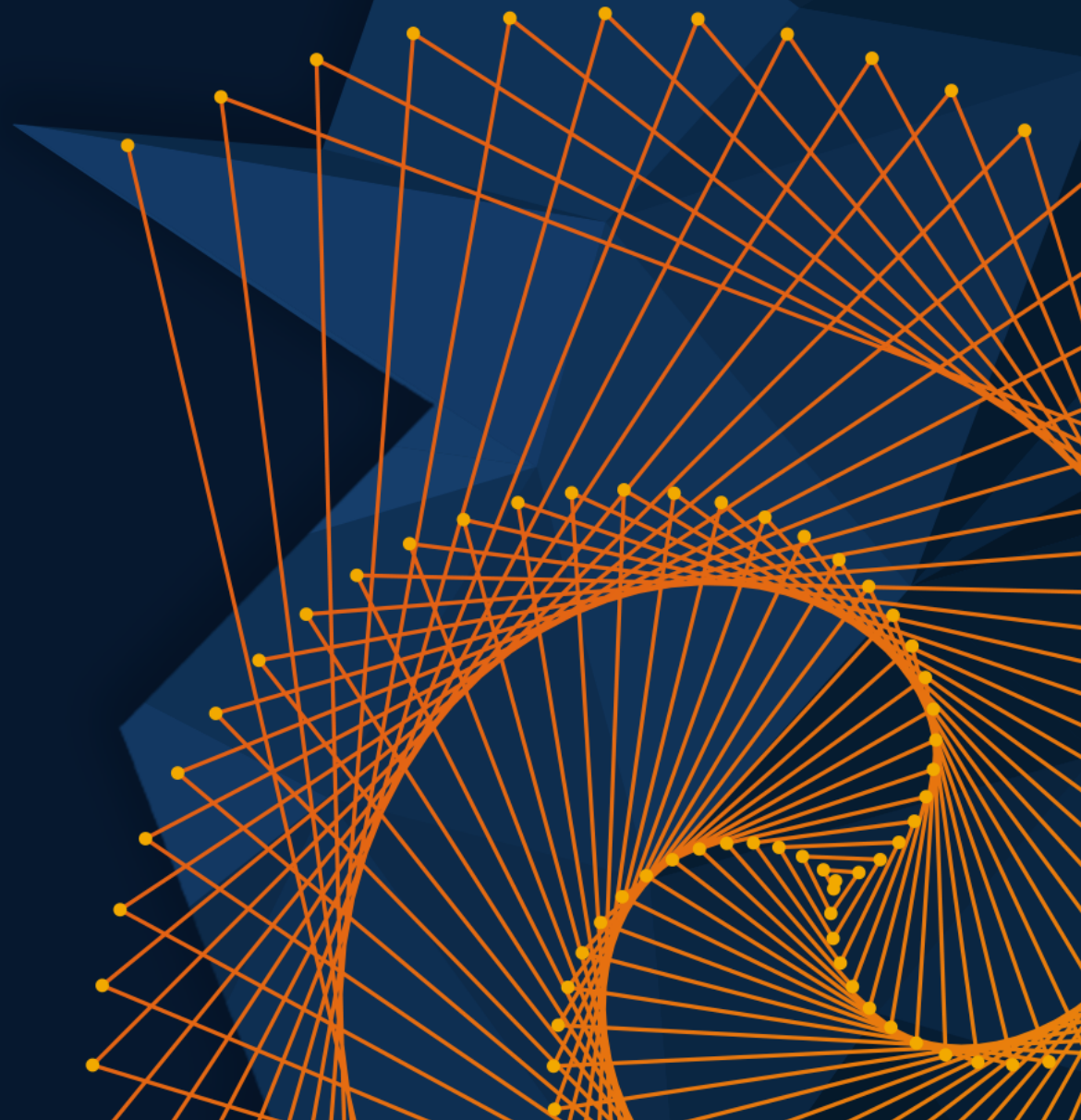
- Using HDL Coder from MathWorks *with* AMD Vitis Model Composer enables users to target all the programmable engines on Versal from a single Model-Based Design environment

For More Information

1. Visit **MathWorks.com/AMD** for more information on targeting workflows for AMD Adaptive FPGAs and SoCs

2. Contact **fpga_expert@mathworks.com** if you want to evaluate this workflow using HDL Coder with AMD Vitis Model Composer

MATLAB EXPO



MathWorks®